Project Completion Report:

Project Title:

"To Study the Impact and Compensation of Process-Induced Variations in Junctionless Transistor for Improved Reliability"

Start-Up Research Grant (Young Scientists)
Science and Engineering Research Board (SERB)
Government of India

No. SB/FTP/ETA-268/2012
Sanctioned Date: 03/09/2013 for 3 years

Submitted by

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Contents

1. Bank Draft of Rs. 32,947/- of unutilised amount.
   (Draft No: 048806 dt. 10.03.2017, SBI, Tezpur University Brance)

   Unutilised amount under Non-Recurring Head: Rs. 11,905/-

   Unutilised amount under Recurring Head : Rs. 21,042/-

   .....

   Total unutilised amount : Rs. 32,947/-
   (Rupees thirty two thousands nine hundreds forty seven only)

2. Statement of expenditure (two copies)
3. Utilisation Certificate for Non-Recuring Grants (Financial year wise)
4. Utilisation Certificate for Recuring Grants (Financial year wise)
5. Project Completion Report

22/03/2017

(DR. RATUL KUMAR BAROAH)

Annexure-IX

PROJECT COMPLETION REPORT

Notes:
1. The PCR should be in bound form.
2. Cover page should include the title of the project, file number, names and addresses of the investigation.

1. Title of the project: **To study the impact and compensation of process-induced variations in junctionless transistor for improved reliability**

2. Principal Investigator: Dr. Ratul Kumar Baruah

3. Implementing Institution(s) and other collaborating Institution(s): Tezpur University

4. Date of commencement: 03/09/2013

5. Planned date of completion: 02/09/2016 (3 years)

6. Actual date of completion: 02/09/2016

7. Objectives as stated in the project proposal:

   (a) To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability.
   (b) Circuit Design using Junctionless transistor

8. Deviation made from original objectives if any, while implementing the project and reasons thereof:

   The first part of the objective was completed. In second part, small circuits like current course amplifiers were designed and simulated.

9. Experimental work giving full details of experimental set up, methods adopted, data collected supported by necessary table, charts, diagrams & photographs:

   There was no experimental work involved in the project

10. Detailed analysis of results indicating contributions made towards increasing the state of knowledge in the subject:

    A separate document on "Project Report" of detailed analysis of results indicating contributions is attached at the end.

11. Conclusions summarizing the achievements and indication of scope for future work:

11.1 Conclusion

Low power and high performance devices are in demand for today's microelectronics market. Recently, junctionless transistor has proven itself as a very promising device in this arena. The first

part of the work discusses about the analog and digital performances; process and temperature effects of a double-gate junctionless transistor. In the second part, effects of well bias are utilized to improve the hot carrier effect of a bulk planer junctionless transistor. In the last part an analytical channel potential model for shorter-channel double gate junstionless transistor (DGJLT) is developed.

It is observed that

- Double-gate JLT show better device performance characteristics in terms of SCEs, transconductance to drain current ration and intrinsic gain compared to its similar dimension inversion mode (IM) counterpart and later device outperforms in terms of speed.
- DGJLT electrical parameters are more immune to channel length variations. However, there is a notable threshold voltage change of the device with silicon thickness compared to a junction based (JB) device.
- Unlike JB MOSFET, overall performance of a DGJLT is not degraded much by increase in temperature and use of high-k gate dielectrics.
- The effects of well bias are utilized to improve the hot carrier effect of a bulk planer junctionless transistor. Though positive well bias helps in improving hot carrier effect; threshold voltage (V_T) decreases and subthreshold slope (SS), drain induced barrier lowering (DIBL) increases with forward well bias (V_W) for different values of channel length (L), channel thickness (Tsi), gate oxide thickness (Tox) with almost similar trend. Well doping concentration helps in improving the OFF-state current (I_{OFF}) of the device at the cost of slight ON-state current (I_{ON}) degradation which however increases I_{ON}/I_{OFF} ratio. There is more V_T decrease with an increase in well bias for higher temperature. Well bias thus can be used to set the threshold voltage at any desired value.

11.2 Future Scope of the Work

The findings presented in this work are mostly based on the simulation results including appropriate models. This helped us to arrive at a qualitative understanding of the device operation. More rigorous information can be obtained by full quantum simulations using either non-equilibrium green's function (NEGF) approach or Wigner-function approach. There is lot of scope for compact modelling for circuit simulation of shorter channel length JLT which includes all short channel effects like hot carrier effect, velocity saturation effect, drain induced barrier lowering effect etc and process induced variation parameters. Designing circuits including process induced variation parameters for low power applications is a fine scope of work. Also, implementation of the working models in spice simulator for circuit simulation is another scope for extending the

work. Studying the reliability issues in DGJLT and developing compact models with reliability issues in the model is excellent scope of research.

12. S&T benefits accrued:

i. List of Research publications

Journals

SN	Authors	Title of paper	Name of the Journal	Volume	Pages	Year
1	**Ratul Kr. Baruah**, Roy P. Paily	A surface-potential based drain current model for short-channel symmetric double-gate junctionless transistor	Journal of Computational Electronics	15	45–52	2016
2	**Ratul Kr. Baruah**, Roy P. Paily	Silicon Carbide based Double-gate Junctionless Transistor for High Temperature Applications	Journal of Electronic Materials	Under Review		

Conferences

[3] **Ratul Kr. Baruah**, Roy P. Paily, "Impact of Active Well Biasing on Process-Induced Variations of a Bulk Planer Junctionless Transistor", ICEE 2016, Dec. 27-30, IIT Bombay

[4] Rekib Uddin Ahmed and **Ratul Kr. Baruah**, "Modeling of Potential and Threshold Voltage in presence of Hot-Carriers for Short-Channel Double-Gate MOSFET", EDCAECT, Oct. 8-10, 2015, Gauhati University, India.

Some other publications in this field that are based on facilities of the said project

[6] **Ratul Kr. Baruah**, Roy P. Paily, "The Effect of High-k Gate Dielectrics on Device and Circuit Performances of a Junctionless Transistor", Journal of Computational Electronics, Springer, vol. 14, no. 2, pp. 492–499, 2015.

[7] **Ratul Kr. Baruah**, Roy P. Paily, "A Dual-Material Gate Junctionless Transistor using high-k spacer for Enhanced Analog Performance", IEEE Transactions on Electron Devices, vol 61, no. 1, pp. 123–128, 2014.

ii. Manpower trained on the project
   a) Research Scientists or Research Associates: Nil
   b) No. of Ph.D. produced: Nil
   c) Other Technical Personnel trained: M.Tech project students were trained through this project

iii. Patents taken, if any: Nil

13. Financial Position:

No	Financial Position/ Budget Head	Funds Sanctioned	Expenditure	% of Total cost
I	Salaries/ Manpower costs	Nil	Nil	Nil
II	Equipment	Rs. 9,85,000/-	Rs. 9,73,095/-	76.14
III	Supplies & Materials	Rs. 30,000/-	Rs. 24,607/-	1.92
IV	Contingencies	Rs. 60,000/-	Rs. 60,000/-	4.7
V	Travel	Rs. 60,000/-	Rs. 59,559/-	4.66
VI	Overhead Expenses	Rs. 1,76,000/-	Rs. 1,60,792/-	12.58
VII	Others, if any	---	---	---
	Total	Rs. 13,11,000/-	Rs. 12,78,053/-	100%

14. Procurement/ Usage of

Equipment a)

S No	Name of Equipment	Make/Model	Cost (FE/ Rs)	Date of Installation	Utilization Rate (%)	Remarks regarding maintenance/
1	ATLAS TCAD Simulation Software	TCAD OMNI License	Rs. 8.98 Lakhs	December 1, 2013	100%	Well Maintained
2	Desktop Computer	HP Pro 6300MT/P3 330M Intel I7-3770	Rs. 66,045 /-	1st December 2013	100%	Well Maintained
3	Scanner	HP G3110	Rs. 9,050 /-	1st December 2013	100%	Well Maintained

b) Plans for utilizing the equipment facilities in future

The TCAD OMNI License from Silvaco is not a perpetual license. The duration of the license is for three years only and it is already over. The Desktop Computer and Scanner will be used for academic purposes.

Name and Signature with Date:

22/03/2017

Assistant Professor
Department Of Electronics & Comm. Engg.
Tezpur University

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(Principal Investigator)


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Annexure-II

ANNUAL INSTALMENT WITH UP-TO-DATE STATEMENT OF EXPENDITURE

(Two copies)

1. SERB Sanction Order No and date: SB/FTP/ETA-268/2012 dated 03/09/2013
2. Name of the PI : Dr. Ratul Kumar Baruah
3. Total Project Cost : Rs. 13,62,000 /-
4. Revised Project Cost (if applicable) : N/A
5. Date of Commencement : 21/09/2013
6. Statement of Expenditure
   (month wise expenditure incurred during current financial year)

1. Grant received in each year:

   a. 1st Year : Rs. 11,11,000 /-

   b. 2nd Year: Nil
   c. 3rd Year: Rs. 2,00000 /-
   d. Interest, if any: Nil

   e. Total (a+b+c+d): Rs. 13,11,000 /-

Month & year	Expenditure incurred/ committed
Year: 2013-2014 (21/09/2013-31/03/2014)	
November (2013)	Rs. 47,291 /-
January (2014)	Rs. 3,684 /-
February (2014)	Rs. 8,98,000 /-
March (2014)	Rs. 78,278 /-
Sub-Total (2013-2014)	**Rs. 10, 27,253 /-**
Year: 2014-2015 (01/04/2014-31/03/2015)	
October (2014)	Rs. 5,152 /-
December (2014)	Rs. 3,630 /-
January (2015)	Rs. 5,324 /-
Sub-Total (2014-2015)	**Rs. 14,106 /-**
Year: 2015-2016 (01/04/2015-31/03/2016)	
April (2015) April (2015) October (2015) January (2016)	Rs. 9,050 /- Rs. 7,185 /- Rs. 56,643 /- Rs. 1,06,204 /-
Sub-Total (2015-2016) Till 31.03.16	Rs. 1,79,082 /-
Expenditure (1ST April 2016 to End) June (2016) August (2016) August (2016) October	 Rs. 22,750 /- Rs. 7,050 /- Rs. 17,422 /- Rs. 10,390 /-
Sub-Total (April 1, 2016 Till End	Rs. 57,612 /-
Total Expenditure from DOS till End of Project	Rs. 12,78,053/-

Statement of Expenditure

DOS (21.09.2013) to 31.03.2014, 1.04.2014 to 31.03.2015, 01.04.2015 to 31.3.2016 and 1.4.2016 to 02.9.16

Sr No (I)	Sanctioned Heads (II)	Total Funds Allocated (indicate sanctioned or revised) (III)	Expenditure Incurred				Total Expenditure till.. (VII = IV + V + VI)	Balance as on (date) (VIII = III – VII)	Requirement of Funds upto 31st March next year	Remarks (if any) Committed Exp.
			1st Year (DOS 21.9.2013 to 31st March 2014) (IV)	2nd Yr (1st April 2014 to 31st Mar 2015) (V)	3rd Year (VI)					
					1st Apr '15 to 31st Mar '16	1st April '16 2/9/16				
1.	Equipment	Rs. 9,85,000/-	Rs. 9,64,045/-	Nil	Rs. 9,050/-	Nil	Rs. 9,73,095/-	Rs. 11,905/-	Nil	
	Sub-total (A) (Non-Recurring)	*Rs. 9,85,000/-*	*Rs. 9,64,045/-*	*Nil*	*Rs. 9,050/-*	*Nil*	*Rs. 9,73,095/-*	*Rs. 11,905/-*		
2.	Manpower costs	Nil								
3.	Consumables	Rs. 30,000/-	Nil	Nil	Rs. 7,185/-	Rs. 17,422/-	Rs. 24,607/-	Rs. 5,393/-	Nil	
4.	Travel	Rs. 60,000/-	Nil	Nil	Rs.60,000/-	Nil	Rs.60,000/-	Nil	Nil	
5.	Contingencies	Rs. 60,000/-	Rs. 3,684/-	Rs. 14,106/-	Rs. 21,769/-	Rs. 20,000/-	Rs. 59,559/-	Rs. 441/-	Nil	
6.	Others, if any	Nil								
7.	Overhead expenses	Rs. 1,76,000/-	Rs. 59,524/-	Nil	Rs. 81,078/-	Rs. 20,190/-	Rs. 1,60,792/-	Rs.15,208/-	Nil	
	Sub-total (B)	*Rs. 3,26,000/-*	*Rs. 63,208/-*	*Rs. 14,106/-*	*Rs.1,70,032/-*	*Rs. 57,612/-*	*Rs. 3,04,958/-*	*Rs. 21,042/-*		
8.	*Total (A+B) (Recurring)*	Rs. 13,11,000/-	Rs. 10,27,253/-	Rs. 14,106/-	Rs.1,79,082/-	Rs. 57,612/-	Rs. 12,78,053/-	Rs. 32,947/-	Nil	

Name and Signature of Principal Investigator:

Dr. Ratul Kumar Baruah

Date: 24/02/2017

* DOS – Date of Start of project

Signature of Competent financial authority: _____

(with seal) Finance Officer Date: _____

Tezpur University

Note:

1. Expenditure under the sanctioned heads, at any point of time, should not exceed funds allocated under that head, without prior approval of SERB i.e. Figures in Column (VIII) should not exceed corresponding figures in Column (III)
2. Utilisation Certificate (Annexure III) for each financial year ending 31st March has to be enclosed along with request for carry-forward permission to the next financial year.

Unutilised Amount Refunded.
Draft no.: 048806 dtd 20.03.2017 (Rs. 32,947/-)

Project Report on the Title

To Study the Impact and Compensation of Process-Induced Variations in Junctionless Transistor for Improved Reliability

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Submitted by

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Contents

Nomenclature

BJT	Bipolar junction transistor
BPJLT	Bulk planar junctionless transistor
BTBT	Band to band tunnelling
CLM	Channel Length Modulation
CMOS	Complementary metal oxide semiconductor
DIBL	Drain induced barrier lowering
DGJLT	Double-gate junctionless transistor
DGMOS	Double-gate metal-oxide-semiconductor
DRAM	Dynamic read only memory
EOT	Effective oxide thickness
GAA	Gate all around
Ge/Si	Germanium/Silicon
IM	Inversion mode
ITRS	International Roadmap for Semiconductors
JB	Junction based
JLT	Junctionless transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
Mug-FET	Multiple-gate field-effect transistor
RF	Radio frequency
SCE	Short channel effects
SEM	Scanning electron microscope
SOI	Silicon on insulator
SS	Subthreshold swing
SP	Spacer
TCAD	Technology Computer Aided Design
TFET	Tunnel field-effect transistor

Chapter 1

Introduction

Fully depleted (FD) silicon on insulator (SOI) MOSFETs are very promising candidates for sub 100 nm ultra large scale integration (ULSI) because it is suitable for low power and high performance applications. However, it demands (1) ultra-thin semiconductor films (2) elevated source and drain, to reduce series resistance and (3) mid-gap gate, to balance the lowering of threshold voltage. Also, another lapse of the FD-SOI is the field penetration beneath the channel from source and drain through buried oxide (BOX) and substrate, at higher drain voltages. Multigate silicon-on-insulator (SOI) MOSFETs (Mug-FETs) have come into picture for further downscaling of MOSFETs, as these devices have more control on the electrostatics of the channel region because of the more number of gates. Also, Mug-FETs which do not need high channel doping concentration, improve SCEs, increase the carrier mobility and reduce the device variability coming from random dopant fluctuations. Also, Mug-FETs improve SCEs by scaling the thickness of the channel rather than scaling the oxide dielectric. Therefore, gate tunneling current can also be reduced. Because of the above advantages, Mug-FETs are predicted as a successor of planar transistors by the International Roadmap for Semiconductors (ITRS) since 2001 [3]. Unfortunately, in sub-20 nm era, the channel region is not only controlled by the gate but rather by the undesired source and drain regions. Thus, even though SCEs are reduced to some extent, it is not nullified even in with Mug-FET. Very abrupt source and drain junctions requirement of these ultra-short length devices put challenges in doping profile techniques. For example, a typical n-channel MOSFET has doping concentration of 10^{20} cm^{-3} in the source/drain region and $10^{15}cm^{-3}$-10^{16} cm^{-3} in the channel region. Now, to form a junction within a nanometer or fraction of a nanometer or so (theoretically abruptly), with few orders of concentration gradient, is extremely tedious and needs technology breakthrough because of the restrictions in laws of diffusion and statistical nature of the distribution of the doping atoms. Also, very high thermal budget is involved with this process. Flash annealing techniques are now used for heating silicon for a very short duration to minimize diffusion. However, even in total absence of diffusion, ion implantation and other doping techniques cannot achieve perfectly abrupt junctions with many orders of concentration gradient [10]. Thus, even with Mug-FETs, the material and/or device properties have reached fundamental limits in deca-nanometer era [11-13]. Also, SCEs make transistors slower by lowering the maximum switching speed. Tunnel FET (TFET) is studied

extensively because it offers ultra-small SCEs; however it has low ON-state current [14-15]. Single-electron transistor [16] and carbon nanotube [17-18] have been extensively studied as an alternative to conventional transistors in sub-20 nm regime. However, with present available technology, they are rather complicated to fabricate cost effectively for commercial use.

1.1 Junctionless Transistor (JLT)

The existing metal-oxide-semiconductor field-effect transistors are composed of pn junctions in the source-channel-drain path. The pn junctions allow or block current through it according to the applied bias on the gate. Junctionless transistor (JLT), which does not have pn junction in the source-channel-drain path (Fig. 1.1), has recently been reported by Colinge's group at Tyndall National Institute, University College Cork, Ireland [26] following the idea of the first transistor by Julius Edgar Lilienfield in 1925 [27-28]. Lilienfield patented his work under the title "Device for controlling the

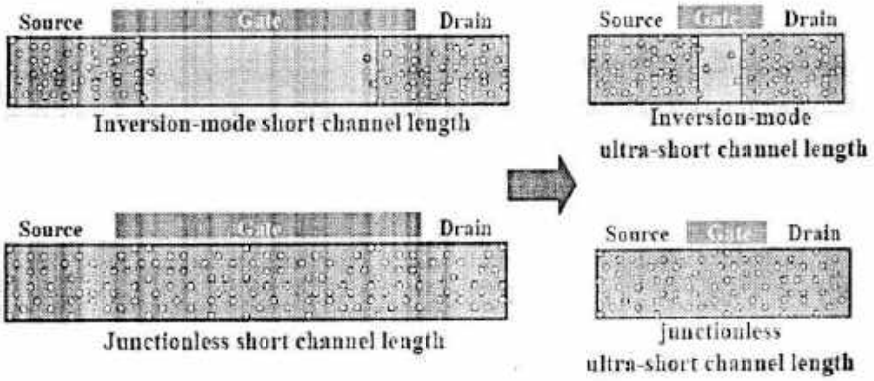


Figure 1.1: Source and drain doping of inversion-mode and junctionless transistor with short channel and ultra-short channel. This Fig. is taken from [9].

electric current". It consists of a thin semiconductor film deposited in a thin insulator layer, itself deposited in a metal electrode (gate). Thus, it does not have a junction; rather it is a simple "registor". It is also called "gated trans-resistor". In principle, current flows in the registor in the same way that drain current flows from drain to source in a MOSFET. Junctionless transistor is basically an accumulation mode device with a very thin silicon thickness (~5-10 nm). The requirement of thin semiconductor layer is to have full depletion of carriers when the device is turned off. Therefore, JLT offers good subthreshold characteristics. However, a typical accumulation mode device is made in relatively thick silicon films (typically higher than 20 nm or so) and hence it exhibits worst short channel performances. However, one advantage of accumulation mode transistor is, drain current varies less with channel doping concentration. The other major difference of JLT with accumulation

mode transistor is that in the former, accumulation of carriers happens at a higher threshold voltage than the later device. The junctionless transistor which is also called "gated resistor" or "nanowire pinch-off FET" is highly doped (typically ~8×10^{18} cm^{-3} to 8×10^{19} cm^{-3}) to have an acceptable threshold voltage. Commonly, a junctionless transistor has same doping concentration at source, channel and drain regions. Thus, the structure of a JLT is $N^+ - N^+ - N^+$ for n-channel and $P^+ - P^+ - P^+$ for p-channel in the source-channel-drain region. P^+ and N^+ polysilicon gates are used for n and p channel JLT respectively (N^+/ P^+ denote highly doped with N/P-type dopants respectively). However, non-uniform doping in JLT has also been reported; to obtain superior ON-state to OFF-state current ratio (I_{ON} /I_{OFF}) compared to uniformly doped JLT [29].

JLTs have many advantages over conventional MOSFETs such as – better SCE performance (reduced drain induced barrier lowering (DIBL) and subthreshold slope (SS) degradation) resulting better scalability, lesser sensitive to doping fluctuations and negative bias thermal instability, greatly simplified process flow and low thermal budgets after gate formation resulting in flexibility in the choice of materials for gate dielectric and gate metal etc. [26, 30-32]. Because of uniform and homogeneous doping in the channel region, a JLT eliminates the subsequent annealing process and the device can be fabricated with shorter channel lengths. In addition, JLTs offer low standby power operation and low gate induced drain leakage [30, 33-34]. Also, lesser fabrication steps reduce process cost significantly compared to junction based devices of similar dimension [35]. JLTs exhibit lesser random telegraph-noise [36] and 1/f noise [37]. JLT has fully CMOS compatibility. With constant device dimensions scaling, the effective gate oxide thickness decreases. This increases vertical electric field according to Takagi et al.'s relation $\mu \approx E^{-0.3}$ [38-39]. The inversion carrier mobility in a conventional MOSFET is reduced because of vertical electric field. For example when technology node changes from 0.8 μm to 0.13 μm, mobility decreases from 400 to 130 cm^2/V. The vertical electric field in a JLT is much lower compared to junction based MOSFET and accumulation mode devices as discussed below. Therefore, mobility in a JLT is not reduced much because of vertical electric field [40]. The conventional junction based device is normally an OFF device, as the drain junction is reverse biased. It prevents current flowing through the device. To turn the device on, an inverted channel is created by applying a gate bias. However, a JLT is normally an ON-device. The workfunction difference between the gate electrode and silicon nanowire (~1.1 eV) shift the flatband voltage and turns the threshold voltage into a positive value. In the ON-state, the device is in flatband condition. Therefore, there is zero vertical electric field perpendicular to the urrent flow. Unlike in a junction based transistor where conduction mechanism is surface based; in a JLT, current basically flows through bulk conduction mechanism. The threshold voltage depends on doping, equivalent oxide thickness as well as on the width and thickness of the nanowires [41]. In a JLT, the OFF-state current is determined solely by the electrostatic control of the gate and not by the leakage current as is the case for junction based device. This makes JLT lesser sensitive to contamination [30].

Junctionless transistor is studied theoretically with single, double, triple and gate-all-around architectures; and fabricated with triple and gate-all-around architectures. Fig. 1.4 (a) shows the schematic of first fabricated nanowire transistor (Trigate structure) along with (b) transmission electron micrograph (TEM) of silicon gated resistor nanoribbons of five parallel devices with a common polysilicon gate electrode [26].

However, along with the many advantages that junctionless transistor offers as aformentioned, it has some disadvantages as well. One of the most important drawback of JLT is it suffer from lesser ON-state current (I_D) and hence transconductance (G_m) compared to inversion mode MOSFETs due to high doping concentration (N_D) in the channel region [42]. Also, to have a highly doped uniform channel with such small thickness (~ 5–10 nm) is extremely challenging and expensive for non planer kind of structure. The higher channel doping concentration to accomplish higher ON-state current makes threshold voltage variation with doping concentration as well as nanowire width [43-44].

Chapter 2

Estimation of Analog, Digital and Low Power Performances of Junctionless Transistor (JLT)

We are in an era where customers of electronic gadgets, always look for low power consumption of the product. So, it is of high concern to operate the device at lower supply voltage. However, there are rare reports on low power operation of JLT. Recently, Ghosh et al. have reported the ultra low-power analog/RF applications of JLT [47]. They found that JLT has much higher performance compared to inversion mode counterpart in regard of analog/RF applications. However, there are no reports on low power operation of JLT for digital applications yet, to best of our knowledge. Here, we report a systematic study for digital performance parameters of a shorter-channel DGJLT at lower supply voltage and performed its comparison with inversion mode counterpart.

2.2 Double-Gate JLT (DGJLT) for Analog Applications

2.2.1 Device Structure and Operation of DGJLT

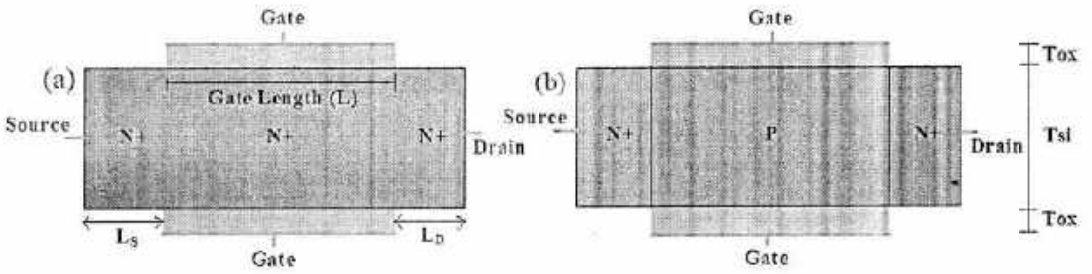


Figure 2.1: Cross-sectional view of n-channel (a) junctionless (DGJLT) (b) conventional inversion mode symmetric double-gate transistor (DGMOS).

Fig. 2.1 (a) and (b) shows the device structures for DGJLT and DGMOS respectively. A DGMOS transistor has two pn junctions i.e., source-gate and drain-gate in source-channel-drain path and an n-type DGMOS has N^+–P –N^+ structure where current conduction is due to the inverted carriers in the

channel region. N^+ means channel is highly doped with boron atoms. A DGJLT has same structure as DGMOS transistor with the exception that there is no pn junction in the source-channel-drain path i.e., an n-channel device has N^+–N^+–N^+ structure and p-channel device has P^+–P^+–P^+ structure. It has uniform doping throughout the source-channel-drain region, where only majority carriers carry the current. Unlike a conventional DGMOS, where the channel is lightly doped or undoped, the channel region of a JLT is highly doped (~8×10^{18}– 8×10^{19} cm^{-3}) to attain an appreciable threshold voltage. A JLT uses P^+ polysilicon as gate material for n-channel device and N^+ polysilicon for n-channel device respectively. Metal gate can also be used as a gate material. For a JLT, the workfunction difference between silicon layer (n-channel region) and metal gate (Φ_{MS}) is given by

$$\Phi_{MS} = \Phi_M - \left(\chi + \frac{E_g}{2} - kT \ln\left(\frac{N_D}{n_i} \right) \right) \tag{2.1}$$

Interface charges are neglected. Where, χ is the electron affinity and E_g is the band-gap energy of silicon, k is Boltzman's constant and T is temperature. N_D and n_i are the channel doping concentration and intrinsic doping concentration respectively. For example, with $N_D=1\times10^{19}$ cm^{-3}, the workfunction difference, Φ_{MS} ~1.12 eV. Therefore, even without any gate bias, the channel region of JLT is fully depleted because of this workfunction difference. For this to happen the channel region of JLT is kept thin. Therefore, current conduction mechanism in JLT is different than inversion-mode and accumulation-mode transistor. In an inversion-mode transistor, with applied gate voltage, the channel is weakly inverted followed by strong inversion of carriers. In accumulation-mode transistor, with applied bias the channel region is depleted followed by accumulation of carriers at the surface. However, for JLT, compared to accumulation-mode transistor, accumulation of carriers at the surface happens at a much higher threshold voltage as shown Fig. 2.2.

In the subthreshold region ($V_{GS} < V_T$), the channel of a DGJLT is fully depleted. For a gate voltage, $V_{GS} > V_T$, the channel is partially depleted. When the gate voltage is equal to the flat band voltage, a completely neutral channel is created and current flows through the centre of the channel by the bulk conduction mechanism. On further increasing the gate voltage, majority carriers are accumulated in the bulk of the channel region, unlike conventional inversion DGMOS transistor, where inverted layer of carriers are formed at the semiconductor–insulator interface [46] Fig. 2.3 shows the band diagram for the DGJLT from fully depleted to accumulation region. The current conditions depending on different gate and drain voltages for a symmetric DGJLT for (a) subthreshold fully-depleted, (b) linear partially-depleted, (c) saturation partially-depleted, (d) linear accumulated, (e) linear accumulated & partially-depleted, and (f) saturation accumulated & partially-depleted are also shown in Fig. 2.4 qualitatively.

In this work 2D numerical device simulations are performed for the devices shown in Fig. 2.1, using Atlas device simulator [48]. The simulations are carried out using two carriers Fermi-Dirac

model without impact ionization to account for highly doped channel. Band-gap narrowing (BGN) and Schottky–Read–Hall (SRH) recombination models are included in simulations. As high-k gate dielectric materials are used, quantum models are not incorporated for gate leakage purpose. The mobility model includes both doping and transverse-field dependence. The technology parameters and the supply voltages used for the device simulations are according to the International Technology Roadmap for Semiconductors (ITRS) guidelines [2]. Uniform n-type channel doping having concentration $N_D = 1.5\times10^{19}$ cm^{-3} for DGJLT and $N_D = 2\times10^{15}$ cm^{-3} for DGMOS are used in this study. Typical value of doping concentration of 1×10^{20} cm^{-3} is used for source/drain extensions of DGMOS. Hafnium oxide (HfO_2, k = 22) is used as a gate oxide material having equivalent oxide thickness (EOT) of 1 nm. For a fair comparison of both the devices, threshold voltage is fixed at 0.25 V corresponding to drain current value of 10^{-7} A at V_{DS} = 50 mV by adjusting the gate workfunction, which are 5.36 eV and 4.8 eV for DGJLT and DGMOS respectively. The drain and source extensions are taken as 20 nm for all simulations. The source and drain extensions (L_S and L_D) are typically assumed to be shorter compared to channel length in order to avoid parasitic resistance effects. But, we have taken such a value of L_S and L_D in order to predict the worse case situation.

2.2.2 Simulation Results and Discussion

Fig. 2.5 shows the electric field distribution of the devices along the channel direction close to the silicon-oxide interface. The electric field distribution is symmetrical in source and drain sides for both the devices at V_{DS} = 50 mV. DGMOS has higher electric field compared to DGJLT in the channel region. When the drain voltage is increased to 1 V, the electric field on the drain side is increased for the devices thereby resulting in an asymmetrical distribution on both sides of the gate as obvious. Compared to DGJLT, the DGMOS has retained higher electric field in the channel region for V_{DS} = 1 V.

Fig. 2.6 shows drain current (I_D) versus gate voltage at V_{DS} = 50 mV and 1 V. DGJLT has lesser leakage current and hence can be scaled to shorter channel lengths compared to DGMOS. Carrier mobility of junctionless transistors is not reduced much due to its lesser scattering. Also, JLT has lower vertical electric field compared to inversion mode transistors in the ON-state [40]. In addition, for a DGJLT, the bulk current drives almost the total current [26] in the saturation region, however in an inversion mode DGMOS, the current is dominated by the surface current component. Therefore, ON-state current of DGJLT is lesser compared to DGMOS although the values are comparable. ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) and subthreshold slope (SS) of a nanowire kind of device

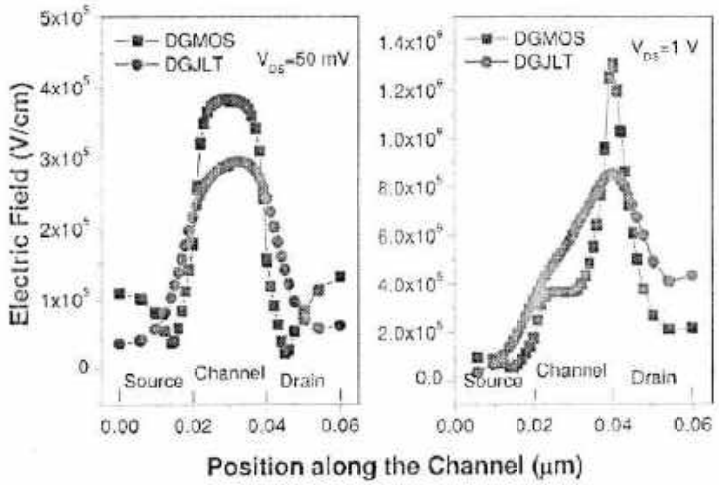


Figure 2.5: Electric field (E) along the channel length at V_{DS}=50 mV (left Fig.) and 1 V (right Fig.). L = 20 nm, T_{si} = 10 nm, EOT = 1 nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

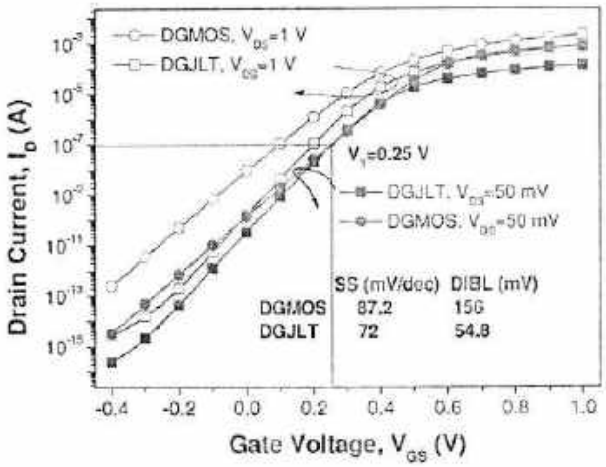
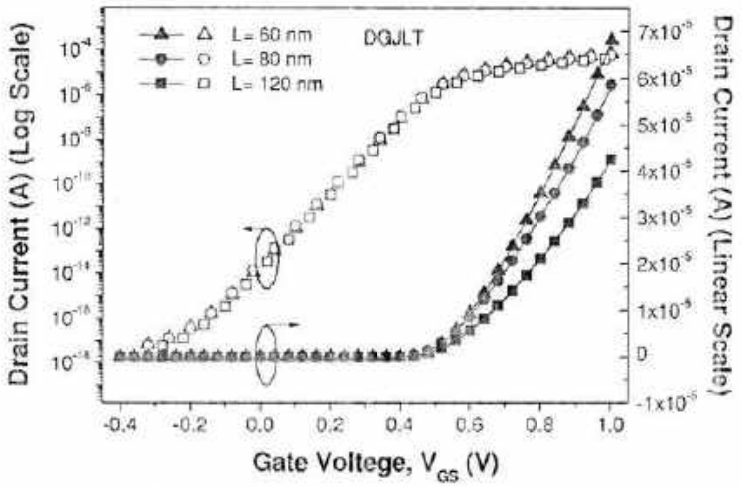
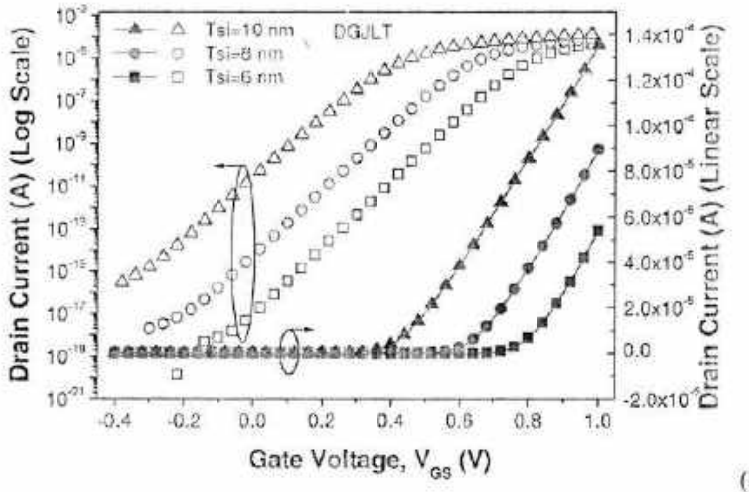


Figure 2.6: Drain current vs. gate voltage at V_{DS} = 50 mV (closed symbols) and 1 V (open symbols). L = 20 nm, T_{si} = 10 nm, EOT = 1 nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

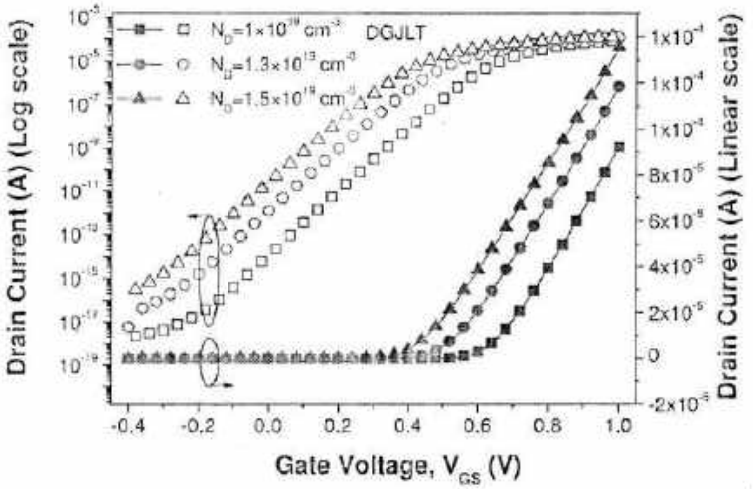
also depends on dimension effects as well. It is reported that nanowires with low diameter and oxide thickness tend to have the best transistor characteristics [49]. The value of SS for DGJLT and DGMOS are 72 mV/dec and 87.2 mV/dec respectively for channel length of 20 nm. SS is defined as the gate voltage shift for one decade change in drain current in subthreshold region. The drain induced barrier lowering (DIBL) value for DGJLT and DGMOS are 54.8 mV and 156 mV respectively for channel length of 20 nm. DIBL is defined as the difference in threshold voltage when the gate voltage is increased from 50 mV to 1 V (DIBL= $V_T(V_{DS} = 50\ mV) - V_T(V_{DS} = 1\ V)$). The lower value of SS and DIBL makes the digital performance better for DGJLT than DGMOS transistor.


L= 60 nm
L= 80 nm
L= 120 nm
DGJLT
Drain Current (A) (Log Scale)
Drain Current (A) (Linear Scale)
Gate Voltege, V_{GS} (V)

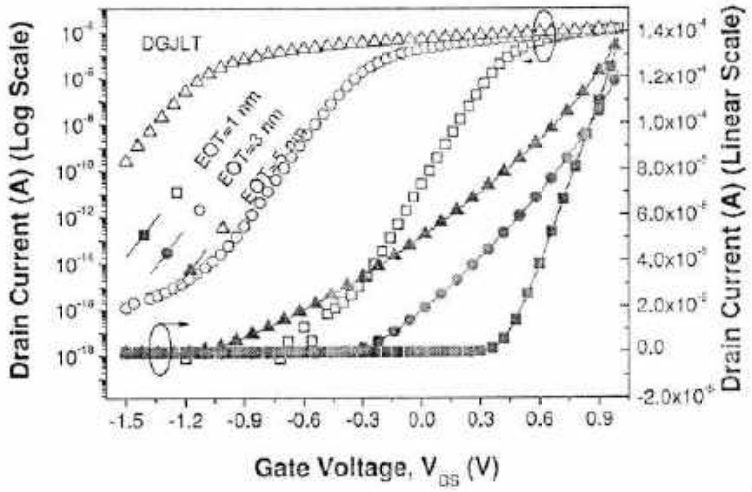
(a)


Tsi=10 nm
Tsi=8 nm
Tsi=6 nm
DGJLT
Drain Current (A) (Log Scale)
Drain Current (A) (Linear Scale)
Gate Voltage, V_{GS} (V)

(b)


N_D=1x10^{19} cm^{-3}
N_D=1.3x10^{19} cm^{-3}
N_D=1.5x10^{19} cm^{-3}
DGJLT
Drain Current (A) (Log scale)
Drain Current (A) (Linear scale)
Gate Voltage, V_{GS} (V)

(c)



(d)

Figure 2.7: Drain current vs. gate voltage of the DGJLT at V_{DS} = 50 mV for (a) different channel lengths, L = 60 nm, 80 nm and 120 nm, while T_{si}, EOT and N_D are kept constant at 10 nm, 1 nm and 1.5×10^{19} cm^{-3} respectively. (b) different channel thicknesses, T_{si} = 6 nm, 8 nm and 10 nm, while EOT, L and N_D are kept constant at 1 nm, 20 nm and 1.5×10^{19} cm^{-3} respectively. Both linear (closed symbols, right y-axis) and log scales (open symbols, left y-axis) are plotted. (c) different channel doping concentrations, $N_D = 1\times10^{19}$ cm^{-3}, 1.3×10^{19} cm^{-3} and 1.5×10^{19} cm^{-3}, while at T_{si}, L and EOT are kept constant at 10 nm, 20 nm and 1 nm respectively and (d) different oxide thicknesses at EOT=1 nm, 3 nm and 5 nm, while T_{si}, L and N_D are kept constant at 10 nm, 20 nm and 1.5×10^{19} cm^{-3} respectively. Both linear (closed symbols, right y-axis) and log scales (open symbols, left y-axis) are plotted.

The drain current dependency on channel length, silicon thickness, channel doping concentration and oxide thickness is investigated for a DGJLT. Fig. 2.7 (a) shows the drain current versus gate voltage characteristics of DGJLT for different channel lengths, L = 60 nm, 80 nm and 120 nm respectively. As expected, drain current is higher for lower channel lengths when all other parameters are kept constant. Fig. 2.7 (b) shows the drain current versus gate voltage characteristics of DGJLT for different silicon thickness, T_{si} = 6 nm, 8 nm and 10 nm respectively. The number of bulk carriers and hence the drain current depends appreciably on the silicon thickness and its value is highest for T_{si} = 10 nm. Fig. 2.7 (c) shows the drain current versus gate voltage characteristics of DGJLT for different channel doping concentrations, $N_D = 1\times10^{19}$ cm^{-3}, 1.3×10^{19} cm^{-3} and 1.5×10^{19} cm^{-3} respectively. Drain current is highest for $N_D = 1.5\times10^{19}$ cm^{-3}. Fig. 2.7 (d) shows the drain current versus gate voltage characteristics of DGJLT for different oxide thickness, EOT = 1 nm, 3 nm and 5 nm. The drain current depends significantly on the oxide thickness and its value is highest for EOT= 1 nm. Similar study for DGMOS is already reported and therefore not discussed here. However, from the

characteristics of both devices, it was observed that the threshold voltage of DGMOS is less sensitive to silicon thickness and oxide thickness variations compared to DGJLT. Nevertheless, the threshold voltage of DGMOS is more sensitive to channel length variation compared to DGJLT.

The transconductance G_m (= $\partial I_D/\partial V_{GS}$) is a figure of merit which indicates how well a device converts a voltage to a current. Though the G_m values are closer for both the devices, at lower gate voltages (V_{GS} < ~ 0.2 V), DGMOS has higher value in the super threshold region as shown in fig. 2.8. The values of G_m for DGMOS and DGJLT are 4.5 mS and 1.9 mS respectively at V_{GS} = 1V. An important figure of merit for analog performance of a device namely, transconductance/drain current ratio (G_m/I_D), also called transconductance generation factor is also plotted with respect to gate voltage, V_{GS} in fig. 2.8 for a drain voltage, V_{DS} of 1 V. The G_m/I_D parameter represents the efficiency of a transistor to convert dc power into ac frequency and gain performance [50]. The values of G_m/I_D for DGJLT and DGMOS are 31.3 V^{-1} and 23.3 V^{-1} respectively at V_{GS} = 0.2 V. A smaller value of SS for DGJLT implies higher G_m/I_D than DGMOS in the subthreshold region. G_m/I_D is mainly controlled by body factor of the devices in weak inversion regime; however its value decreases in moderate/strong inversion regime due to the mobility degradation because of scattering etc. [33].

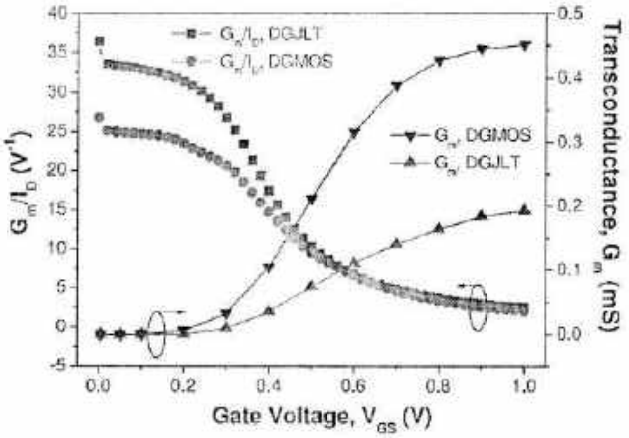


Figure 2.8: Transconductance/drain current ratio (G_m/I_D) and Transconductance (G_m) vs. gate voltage at V_{DS} = 1 V, L = 20 nm, T_{si} = 10 nm, EOT = 1nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

Fig. 2.9 (a) presents the drain current and drain output conductance G_D (= $\partial I_D/\partial V_{DS}$) variation with drain voltage, V_{DS} for a fixed value of V_{GS} = 1 V. The DGMOS carries higher current and hence output conductance than DGJLT due to its higher electric field at V_{DS} = 1 V [refer fig. 2.2]. The value of G_D for DGMOS and DGJLT are 14.7 (kΩ)$^{-1}$ and 2.7 (kΩ)$^{-1}$ respectively at V_{GS} = 0.02 V. Fig. 2.9 (b) presents the output resistance (R_O) with respect to V_{GS}. DGJLT offers much higher value of R_O due to smaller slope in I_D-V_{DS} characteristics as compared to DGMOS. The values of R_O for DGJLT and DGMOS are 5.3×10^9 Ω and 4.6×10^7 Ω respectively at V_{GS}=0.005 V. Early voltage, V_{EA} with

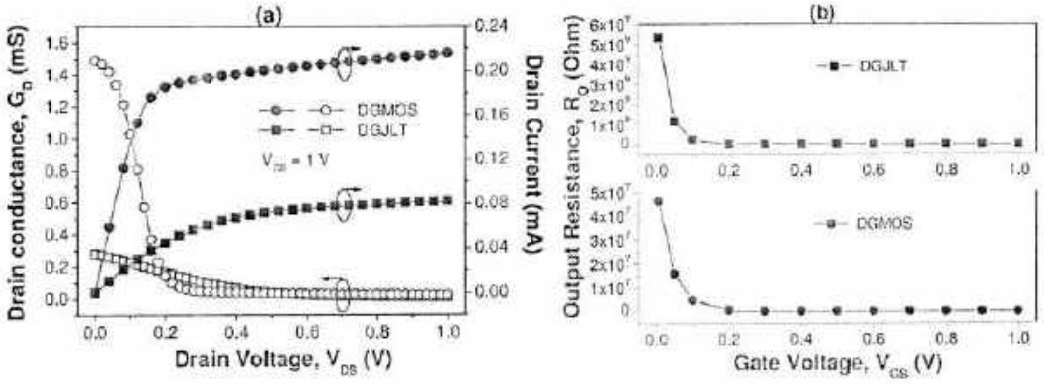


Figure 2.9: (a) Drain output conductance and drain current vs. drain voltage at V_{GS} = 1 V (Left side) (b) Output resistance (R_O) vs. gate voltage at V_{DS}=1 V. L = 20 nm, T_{si} = 10 nm, EOT = 1 nm (right side), N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

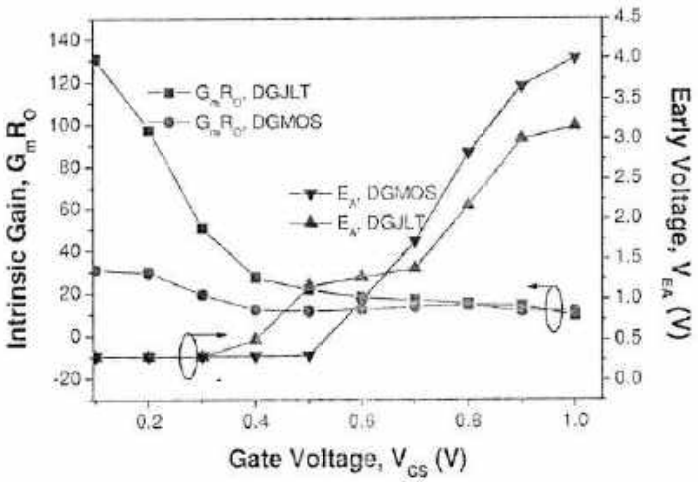


Figure 2.10: Intrinsic gain (G_mR_O) and Early voltage (V_{EA}) with gate voltage at V_{DS}=1 V. L = 20 nm, T_{si} = 10 nm, EOT = 1 nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

respect to V_{GS} is also shown in fig. 2.10. V_{EA} is higher at larger gate voltages as expected from the slope of I_D-V_{DS} characteristics [refer fig. 2.9 (a)]. Early voltage can be derived from output resistance and vice versa as

$$V_{EA} = R_O I_{D(sat)} \tag{2.1}$$

Where, $I_{D(sat)}$ is the saturation current. The intrinsic gain A_V (= G_mR_O) with respect to V_{GS} is also plotted in fig. 2.10. The intrinsic gain of a device can be written as

$$G_mR_O = \frac{V_{EA}G_m}{I_{D(sat)}} \tag{2.2}$$

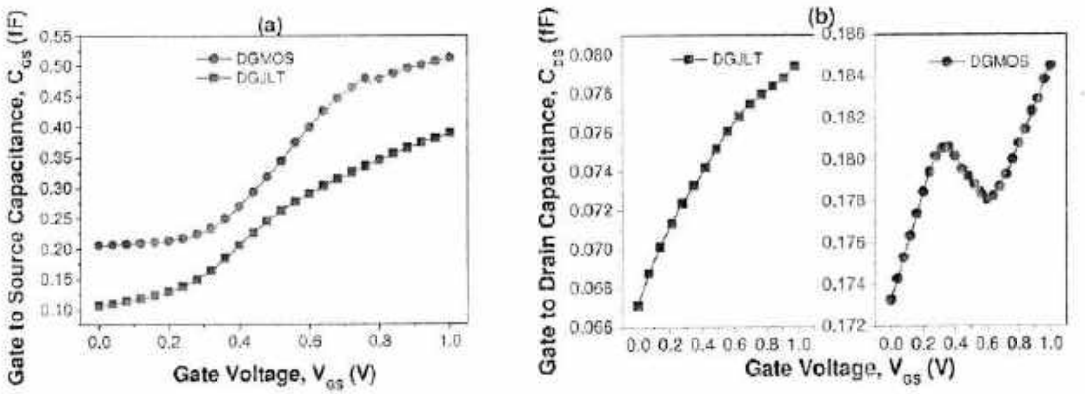


Figure 2.11: (a) Gate to source capacitance (C_{GS}) and (b) Gate to drain capacitance (C_{GD}) vs. gate voltage at V_{DS}=1 V. L = 20 nm, T_{si} = 10 nm, EOT = 1 nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

The gain values for DGJLT and DGMOS at V_{GS} = 0.2 V are 97.4 and 29.7 respectively.

The parasitic capacitance of a device mainly consists of two parts namely oxide generated and junction generated components. As there are no pn junctions in a junctionless transistor in source-channel-drain path, junction related capacitances are not considered in this study. The intrinsic capacitances depend on the operating region of the device. Fig. 2.11 (a) and fig. 2.11 (b) shows the gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances as a function of V_{GS} for V_{DS} = 1 V. All the capacitances are extracted from the small-signal ac device simulations at a frequency of 1 MHz. DGMOS has the higher value C_{GS} and C_{GD} both in the subthreshold and superthreshold region as compared to DGJLT. The gate-to-bulk (C_{GB}) capacitance value for the devices is much lesser than C_{GS} and C_{GD}. DGJLT has higher C_{GB} value as compared to DGMOS (not shown). Higher value of C_{GS} and C_{GD} is due to higher electron concentration in the source and drain side respectively. The unity-gain cut-off frequency (f_T) is another useful figure-of-merit for analog applications. It is given by

$$f_T = \frac{G_m}{2\pi(C_{GS}+C_{GD}+C_{GB})} \tag{2.3}$$

Fig. 2.12 (a) shows the variation of f_T with V_{GS} for V_{DS} = 1V. At lower V_{GS}, f_T is almost same for all the devices due to almost same values of transconductance. The DGJLT has higher value f_T than DGMOS for V_{GS} > ~ 0.45 V. f_T depends on C_{GS}, C_{GD} and G_m. As the G_m value is higher for DGMOS compared to DGJLT especially at higher V_{GS}, f_T is higher for DGMOS compared to DGJLT. With such f_T values, both the devices can meet ITRS guidelines for the specified voltages and dimensions. Our simulations for DGJLT are calibrated with [46] for channel length L = 1 μm, EOT = 7 nm, channel doping concentration N_D = 1×10^{19} cm^{-3}, source/drain extension = 10 nm and device layer thickness of 10 nm at V_{DS} = 50 mV. As shown in fig. 2.12 (b), both the results are closely matched.

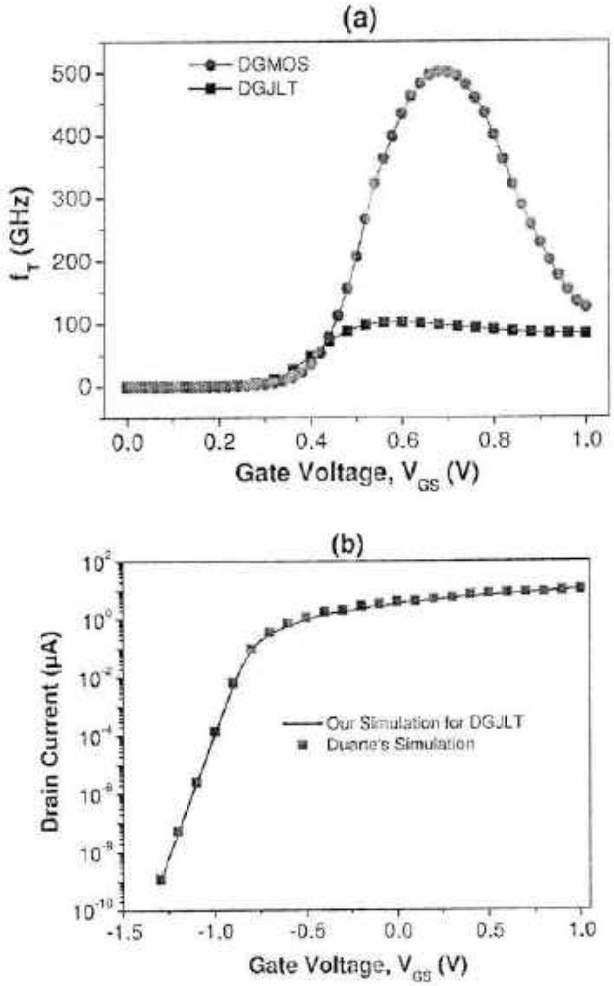


Figure 2.12: (a) Unity gain cut-off frequency (f_T) vs. gate voltage at V_{DS} = 1 V. L = 20 nm, T_{si} = 10 nm, EOT = 1 nm, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS (b) Calibration of our simulated I_D-V_{GS} characteristic for DGJLT with [37] at V_{DS} = 50 mV for L = 1 μm. T_{si} = 10 nm. EOT = 7 nm, N_D = 1×10^{19} cm^{-3}, L_S/L_D = 10 nm.

2.5 Summary

DGJLT offered 1.3 times higher transconductance to drain current ratio at V_{GS} = 0.2 V, 2.9 times higher output resistance at V_{GS} = 0.9 V and 3.3 times higher intrinsic gain at V_{GS} = 0.2 V when compared to a similar DGMOS device. However, in DGMOS, drain current with respect to drain voltage was 2.8 times higher at V_{GS} = 0.9 V and unity gain cut-off frequency was 2.7 times higher at V_{GS} = 0.9 V compared to DGJLT. Among the two devices, DGJLT is more suitable for low frequency, high gain applications while DGMOS is more suitable for high speed applications.

DGJLT presents superior digital performance when compared with the conventional inversion mode DGMOS transistor at low drain voltage also.

Chapter 3

Estimation of Process-Induced Variations and Effect of Temperature in DGJLT

3.1 Introduction

Junctionless transistors (JLTs) have some disadvantages in regard of process variations as described below. Unlike, a conventional MOSFET where channel is either undoped (doping concentration, N_D ~1.5×10^{10} cm^{-3}) or lightly doped (N_D ~10^{15}-10^{16} cm^{-3}), the channel doping concentration of a JLT is much higher (N_D ~8×10^{18}-8×10^{19} cm^{-3}) as mentioned in previous chapter. This high doping concentration in JLT is required to ensure a comparable ON-state current as that of JB counterpart device while maintaining flat band condition at the ON-state to enhance the carrier mobility as a result of reduced surface roughness scattering. For JB device, reduction of channel width (W_{si}) means the channel region is more controlled by the gate. That is, SCE decreases with decrease in W_{si} and hence threshold voltage decreases with undoped or lightly doped channel. However, for JLT because of highly doped channel, threshold voltage is more sensitive to W_{si}. Although Colinge et al. predicted that random dopant fluctuation in junctionless transistors would become small due to its junction free nature [40], comprehensive analysis of threshold voltage fluxtuation caused by random fluxtuation and W_{si} variation is still necessary.

Choi et al. reported the sensitivity of threshold voltage to nanowire width variation for gate-all-around junctionless transistor (GAA JLT) [41]. They found that V_T variation with silicon thickness is more in GAA JLT than IM counterpart. A JLT suffers from more threshold voltage (V_T) variation with random dopant fluxtuations than inversion mode (IM) counterpart [43-44]. A systematic investigation of the other process parameters on electrical performance of JLT is still lacking in literature. In this work, the impact of process induced variations on the electrical characteristics of an n-type junctionless symmetric double-gate transistor (DGJLT) is reported. The process parameters considered here are gate length (L), thickness of silicon film (T_{si}) and gate oxide thickness (T_{ox}). The impact of these process parameters on the electrical parameters viz., ON current, threshold voltage

(V_T) and subthreshold slope (SS) are systematically investigated with the help of extensive device simulations.

At high temperature (T), inversion mode (IM) devices usually would not succeed because of increased subthreshold swing, threshold voltage shift and increased leakage current. However, as the operational principle of JLT is different from IM devices, temperature dependence on the electrical characteristics are expected to be different in JLTs. A JLT has high electric field in the subthreshold region and zero electric field in the ON-state, converse to an IM device. Park et al. reported that JLTs show more marked conductance oscillations at high temperature compared to IM devices [51]. Doria et al. had reported that early voltage and gain are improved with temperature for JLTs unlike conventional MOSFETs. Junctionless transistors show larger threshold voltage variation with temperature than classical MOSFETs though JLT MugFET devices present excellent properties for high temperature applications [33]. Temperature dependence on the digital and analog performance parameters of a DGJLT is systematically investigated with the help of extensive simulations and compared with DGMOS of similar dimensions.

3.2 Process-Induced Variations in the Performance of a DGJLT

3.2.1 Device Structure and Simulation Setup

The device structure for an n-type symmetric DGJLT and DGMOS are shown in Fig. 2.1. Here, threshold voltages of the device having gate length L = 20 nm is fixed at 0.2 V at drain voltage V_{DS} = 1 V which corresponds to drain current of 10^{-7} A by adjusting gate workfunctions which are 5.3 eV for DGJLT and 4.8 eV for DGMOS respectively. The channel doping concentration of DGJLT is considered as 1.5×10^{19} cm^{-3}. For DGMOS, channel and source/drain doping concentration are 2×10^{15} cm^{-3} and 1×10^{20} cm^{-3} respectively. The source and drain extensions (L_S and L_D) are taken as 20 nm. The simulations were carried out using two carriers, the Fermi-Dirac model without impact ionization, doping concentration-dependent carrier mobility and electric field-dependent carrier model. Band gap narrowing model was included. Shockley-Read-Hall (SRH) recombination/ generation were included in the simulation to account for leakage currents.

3.2.2 Simulation Results and Discussion

Fig. 3.1 (a) shows the ON-state current of the devices at channel lengths L = 20 nm to 100 nm at T_{ox} = 1 nm and T_{si} = 10 nm. In all simulations, ON-state current is extracted at a drain voltage of 1 V. The ON-state current for the devices with respect to L follow similar trend. Fig. 3.1 (b) presents the V_T change and SS variation with respect to L at T_{ox} = 1 nm and T_{si} = 10 nm. SS is extracted as the change

in the gate voltage for one decade change in the drain current in the subthreshold region at a drain voltage of 50 mV. Both V_T and SS with respect to L are lower and less fluctuating for JLT than IM transistor as SCEs are improved in such devices due to its junction free nature.

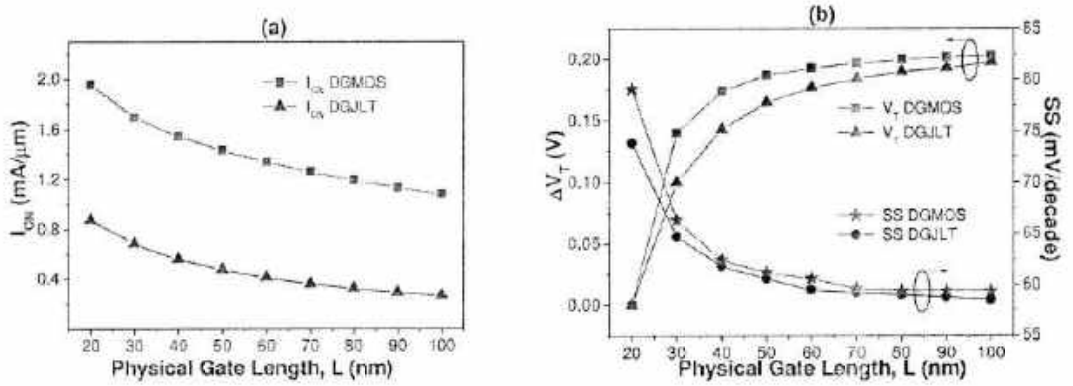


Figure 3.1: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with physical gate length at T_{ox}=1 nm and T_{si}=10 nm, channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

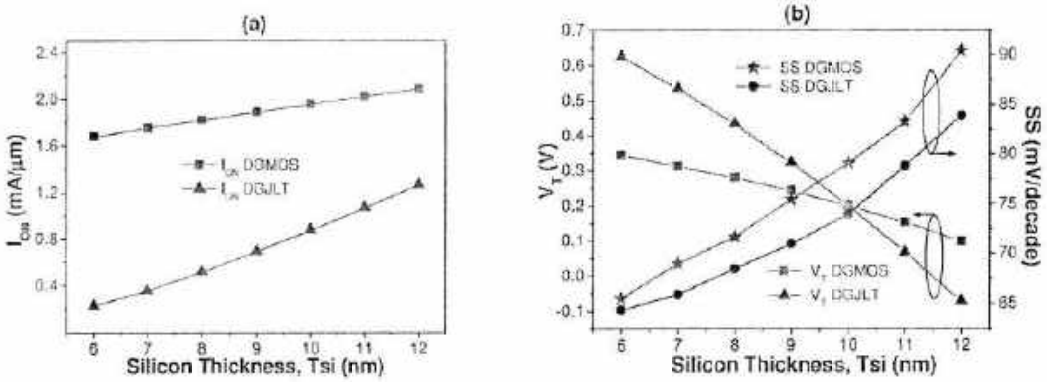


Figure 3.2: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with silicon thickness for L = 20 nm, T_{ox} = 1 nm, channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT, and 2×10^{15} cm^{-3} for DGMOS.

Fig. 3.2 (a) shows the ON-state current of the devices at silicon thickness T_{si} = 6 nm to 12 nm at L = 20 nm and T_{ox} = 1 nm. DGJLT suffers from slightly more ON-state current variation with respect to silicon thickness compared to DGMOS. This is because there is more V_T variation with respect to silicon thickness for DGJLT as compared to DGMOS as will be explained in next figure. V_T and SS variation with T_{si} are plotted in Fig. 3.2 (b) at T_{ox} = 1 nm and L = 20 nm. There is significant variation of threshold voltage variation with respect to silicon thickness for DGJLT than DGMOS. Both the devices follow the almost similar variation of SS with respect to T_{si}. For inversion mode transistors

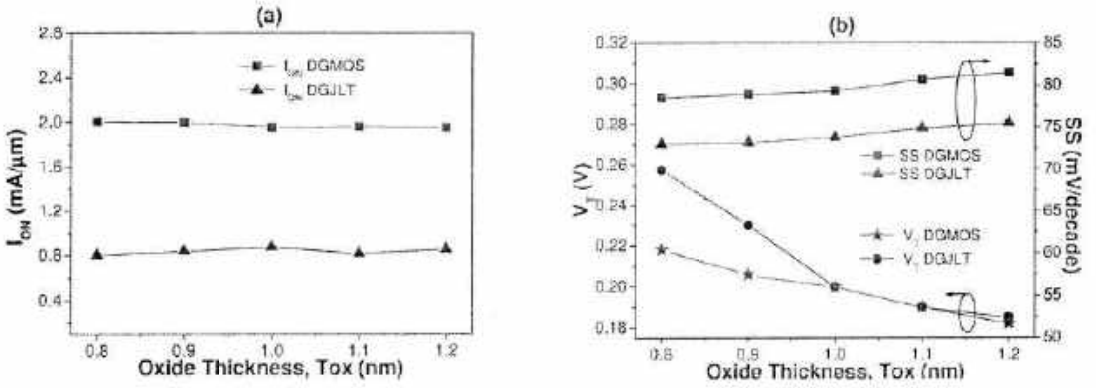


Figure 3.3: (a) I_{ON} and (b) threshold voltage and subthreshold slope variation with gate oxide thickness at L = 20 nm, T_{Si} = 10 nm, channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

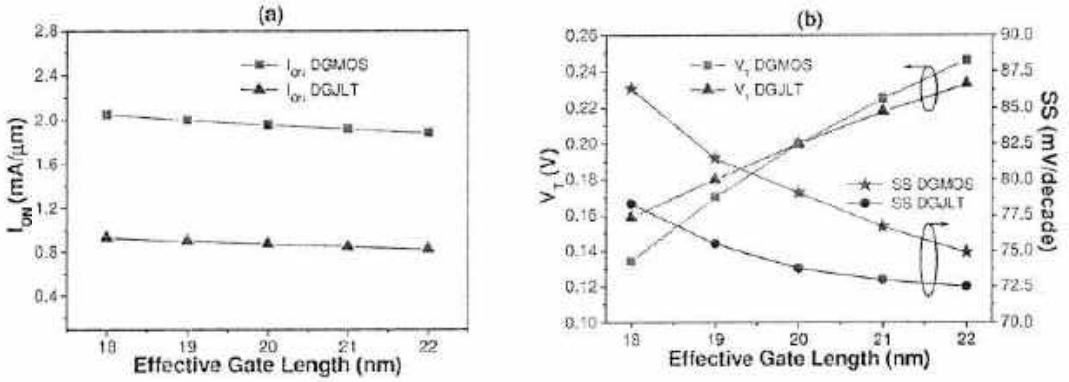


Figure 3.4: (a) I_{ON} and (b) threshold voltage and subthreshold slope with effective gate length at T_{Si} = 10 nm, T_{ox} = 1 nm, channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

there are two trends in the characteristics of V_T versus T_{Si}. One, for low channel doping concentration (10^{15} cm^{-3} to 10^{16} cm^{-3}), SS decreases with increasing T_{Si} and hence V_T decreases. In contrast, with channel doping concentrations greater than 10^{19} cm^{-3} threshold voltage increases with thickness (not shown) [41]. On the other hand, JLT needs a heavily doped channel to ensure a high ON-state current while keeping flat band condition at the ON-state [26, 30]. More sensitivity of V_T in DGJLT may be attributed to the random dopants in highly doped channel in JLT.

Variation of ON-state current with gate oxide thickness is plotted in fig. 3.3 (a) for T_{ox} = 0.8 nm-1.2 nm at T_{Si} = 10 nm and L = 20 nm. For inversion mode transistor, ON-state current decreases very marginally as oxide thickness increases. Because, as T_{ox} increases, gate to source/drain capacitance decreases (C is inversely proportional to T_{ox}) and hence ON-state current increases. However, the

trend is dissimilar for DGJLT. ON-state current marginally increases from T_{ox} = 0.8 nm to 1 nm, after which it deceases slowly. V_T and SS variation with T_{si} are shown in fig. 3.3 (b) at T_{si} = 10 nm and L = 20 nm. SS variation with gate oxide is almost same for DGJLT and DGMOS. Threshold voltage variation with gate oxide is more for DGJLT than DGMOS especially below T_{ox} of 1 nm. When oxide thickness is very thin, gate has more impact on the channel. At higher gate voltage (V_{GS} = 1 V), the random dopant fluctuations is more, which shifts the threshold voltage considering at very lower oxide thickness. The ON-state current variation with effective gate length (L_{eff}) is plotted in fig. 3.4 (a) for L_{eff} = 18 nm-22 nm at T_{si} = 10 nm and T_{ox} = 1 nm. The variation is almost equal for the devices. V_T and SS variation with L_{eff} are plotted in fig. 3.4 (b) at T_{si} = 10 nm and T_{ox} = 1 nm. The variation in V_T and SS with channel length is larger for inversion mode device due to the resistance of the gate overlap/underlap region [52].

3.3 High-Temperature Effects on Device Performance of DGJLT

3.3.1 Device Structure and Simulation Setup

The device structure for an n-type symmetric DGJLT and DGMOS are shown in Fig. 2.1. Threshold voltage of the device is fixed at 0.25 V which corresponds to drain current of 10^{-7} A at drain voltage, V_{DS} = 50 mV at room temperature. The corresponding gate workfunction at this V_T are 5.35 eV for DGJLT and 4.8 eV for DGMOS respectively. The source-channel-drain region has uniform n-type doping concentration (N_D) of value 1.5×10^{19} cm^{-3} for all simulations. HfO_2 is used as gate oxide material having equivalent oxide thickness (EOT) of 1 nm (T_{ox}). The silicon thickness (T_{si}) is taken as 10 nm. The source/drain extensions (L_S/L_D) are taken as 20 nm. Drain voltage is taken as 1 V. The simulations are carried out using two carriers Fermi-Dirac model without impact ionization to account for highly doped channel, band-gap narrowing (BGN) and Schottky–Read–Hall (SRH) recombination models are included in simulations. As high-k gate dielectric materials are used, quantum models are not incorporated for gate leakage purpose. The mobility model includes both doping and transverse-field dependence.

3.3.2 Simulation Results and Discussion

Fig. 3.5 (a) and 3.5 (b) shows the I_D-V_{GS} characteristics of the devices at V_{DS} = 1 V in both linear and log scale. With increase in temperature (T), the threshold voltage decreases and hence the drain current increases for both the devices. In inversion mode (IM) devices, though V_T reduction increases I_D, mobility reduction due to phonon scattering eventually decreases the drain current [79, 80]. At a particular gate voltage of ~ 0.8 V, both these effects compensate each other and it is called the "zero

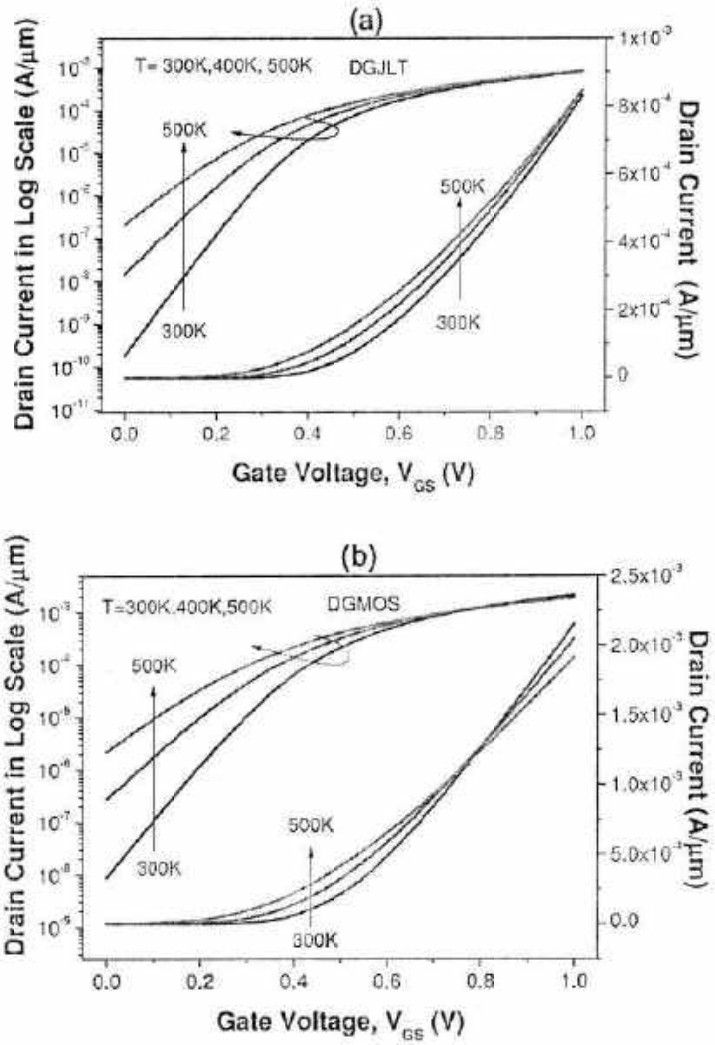


Figure 3.5: I_D-V_{GS} characteristics at various temperatures of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{DS} = 1 V for (a) DGJLT (b) DGMOS. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

temperature coefficient" (ZTC) point. However, in JLTs, reduction in mobility with temperature is much lower than other type of transistors and hence current increases monotonously and there is no ZTC point [42].

Fig. 3.6 shows the ON-state and OFF-state current for the devices at different temperatures at a drain voltage of 1 V. I_{ON} and I_{OFF} are extracted at gate voltage of 1 V and 0 V respectively. I_{ON} is higher for IM devices as compared to JLT due to higher mobility in the former. The ON-state current of DGJLT increases very marginally with increase in temperature till 400 K, after which I_{ON} is almost independent of temperature. Mobility in a highly doped JLT is governed by impurity scattering which varies by $T^{3/2}$ and phonon scattering which varies by $T^{-3/2}$ [53]. Both the effects compensate with each

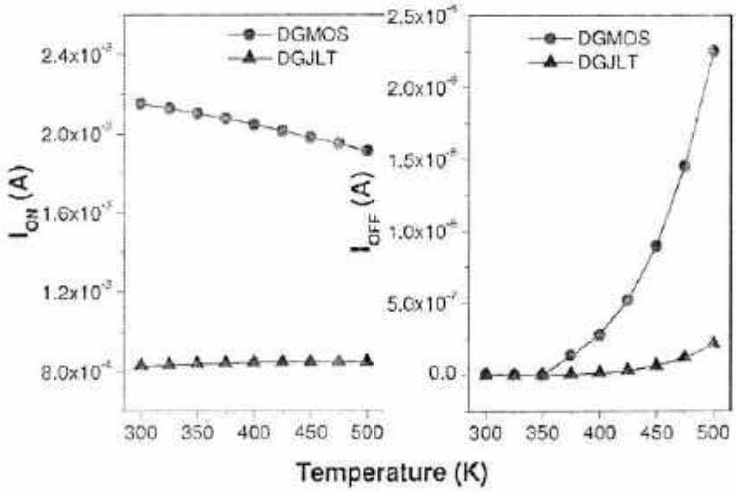


Figure 3.6: I_{ON} and I_{OFF} variation with Temperature of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{DS}=1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

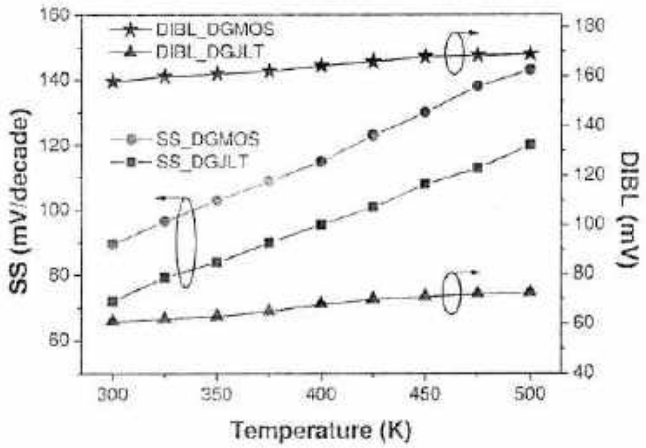


Figure 3.7: Subthreshold slope and drain-induced barrier lowering variation with temperature of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

other and mobility is almost independent of temperature. As expected, ON-state current of DGMOS decreases with increase in temperature due to reduction of surface mobility by phonon scattering. The OFF-state current increases with increase in temperature due to increase in intrinsic carrier concentration n_i. The leakage current increases rapidly with increase in temperature for DGMOS after 350 K. However, for DGJLT, leakage current increases very slowly till temperature of 400 K after which it increases faster. Fig. 3.7 presents SS and DIBL variation as a function of V_{GS} at different temperatures. SS represents the OFF-to-ON switching capability of a device and is defined as the gate voltage which could cause one decade change in drain current in the subthreshold region. DIBL is

extracted as the threshold voltage change when drain voltage shifts from 50 mV to 1 V. Due to junction free nature, JLT offers better SCEs making SS and DIBL lower as compared to inversion mode counterpart as mentioned in previous chapter. As DIBL predicts I_{ON}/I_{OFF} ratio, it is a key parameter for low-voltage CMOS [54]. SS and DIBL increases monotonously with increase in temperature for both the devices. Both SS as well as DIBL variations with temperature are almost similar for the devices.

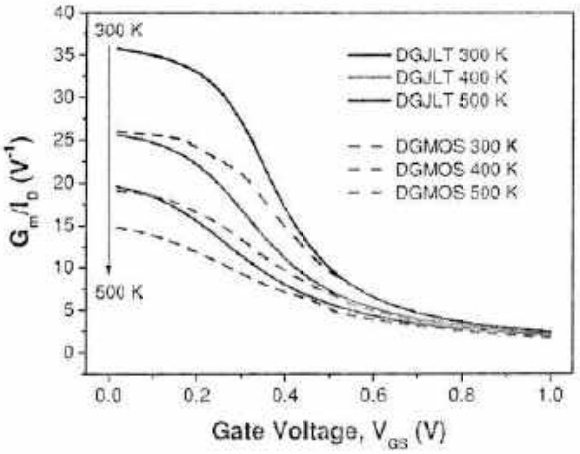


Figure 3.8: G_m/I_D variation with temperature of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{DS} = 1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

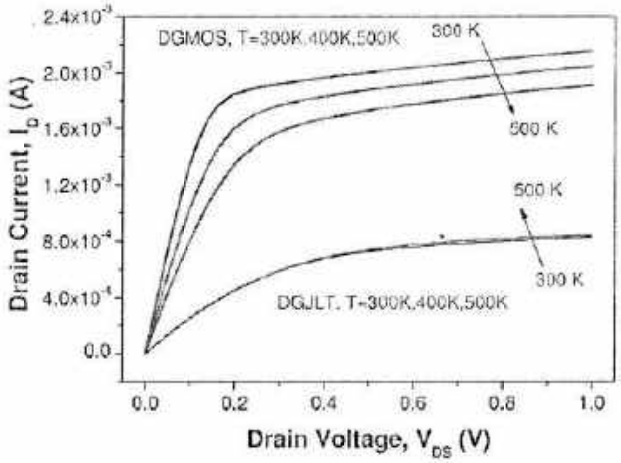


Figure 3.9: Drain current variation with respect to drain voltage at different temperatures of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{GS} = 1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

Fig. 3.8 presents G_m/I_D variation with temperature at V_{DS} = 1 V. In the subthreshold region, G_m/I_D is higher for DGJLT as compared to DGMOS for all temperature ranges because of lower subthreshold

current of the former. G_m/I_D decreases with increase in temperature for both the devices in the subthreshold region. Both show almost similar behaviour because of their similar body factor. When operated at ON-state gate voltage (V_{GS} = 1 V), G_m/I_D of both the devices are independent of temperature. Fig. 3.9 shows the drain current variation with respect to drain voltage at different temperatures for a gate voltage of 1 V. Due to reduction of mobility with increase in temperature, drain current with respect to drain voltage decreases with an increase in temperature for DGMOS.

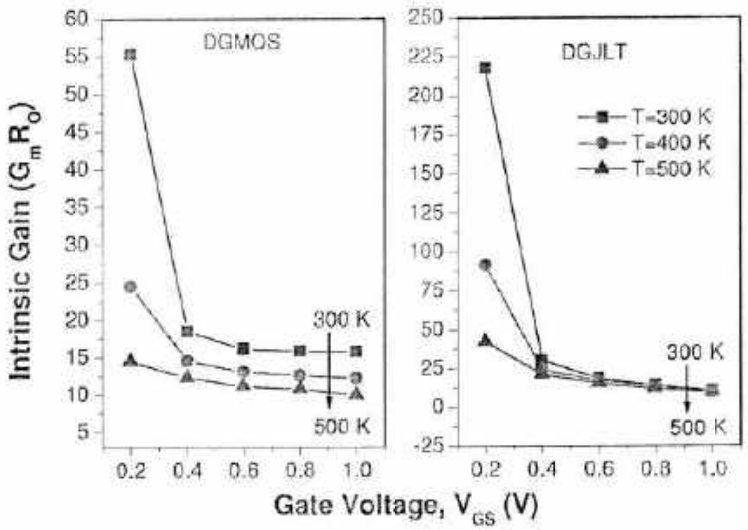


Figure 3.10: Intrinsic gain (G_mR_O) variation with respect to gate voltage at different temperatures of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{DS} = 1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

However, as aforementioned, in JLTs, the mobility is less sensitive to temperature. Therefore, current increases only marginally with increase in temperature. Fig. 3.10 shows the intrinsic gain (G_mR_O) of the devices as a function of gate voltage at a drain voltage of 1 V. G_mR_O decreases with increase in temperature for both the devices; though the change is more for DGMOS compared to DGJLT. As seen from the figure, at a gate voltage greater than – 0.7 V where the device will be actually biased for high frequency operations, the intrinsic gain of DGJLT is almost independent of temperature. This is again due to lesser mobility change in DGJLT as compared to DGMOS. An input sinusoidal small signal with 1 MHz frequency coupled with DC bias is applied to the gate electrode for ac simulations. The gate capacitance C_{GG} (= C_{GS}+C_{GD}) is shown in fig. 3.11. The gate capacitance is lower in JLT as compared to IM devices. In IM devices, the channel is exactly under the gate oxide and gate capacitance is given by W×L×C_{ox} for low V_{DS}. Where C_{ox} is the oxide capacitance and W is the width. However, for a DGJLT, channel is buried in the centre of the silicon layer. Gate capacitance is series combination of C_{ox} and C_{depl}, where C_{depl} is the capacitance of the depletion region between Si-HfO_2 interface and the channel [55]. So, the minimum gate capacitance ($C_{GG\,min}$) can be expressed as

$$C_{GGmin} = \frac{C_{ox}.C_{depl}}{C_{ox} + C_{depl}} \tag{3.1}$$

Lower value of gate capacitance helps in lowering the intrinsic delay of the device. Fig. 3.12 shows the unity gain cut-off frequency ($f_T = G_m / \{2\pi(C_{GS} + C_{GD} + C_{GD})\}$) as a function of gate voltage for different temperatures for both the devices.

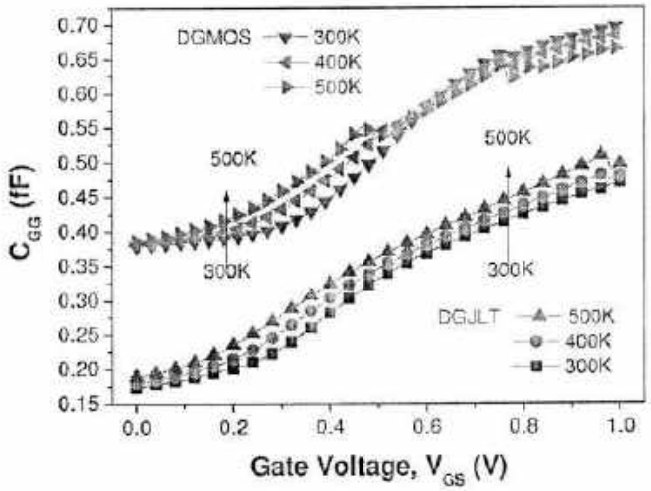


Figure 3.11: Gate capacitance (C_{GG}) as a function of gate voltage at different temperatures of T_{si} = 10 nm, T_{ox} = 1 nm, L = 20 nm at V_{DS} = 1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

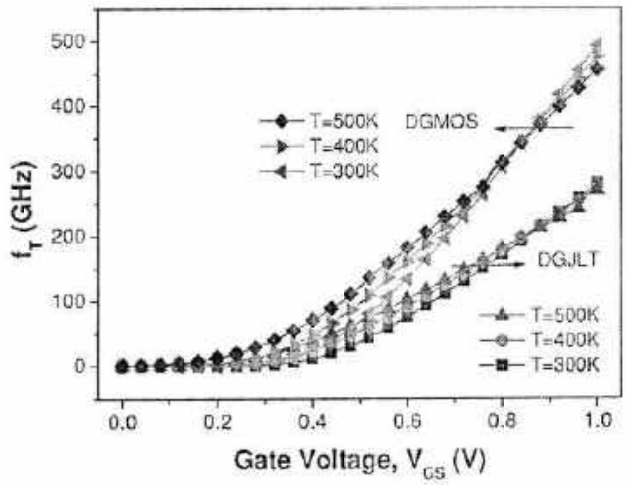


Figure 3.12: Unity gain cuttoff frequency (f_T) as a function of gate voltage at different temperatures of T_{si} = 10 nm. T_{ox} = 1 nm, L = 20 nm at V_{DS} = 1 V. Channel doping concentration, N_D=1.5×10^{19} cm^{-3} for DGJLT and 2×10^{15} cm^{-3} for DGMOS.

f_T is higher for DGMOS as compared to DGJLT because of higher G_m in the former. f_T is higher for higher temperature for both the devices till gate voltage of ~ 0.85 V after which the case is reversed in accordance with aforementioned ZTC point.

3.4 Summary

The effects of variations in process parameters on the electrical characteristics of a junctionless symmetric double-gate transistor (DGJLT) were explored and compared with inversion mode counterpart with the help of extensive device simulations. ON current variation with respect to T_{si} was higher for DGJLT compared to DGMOS. V_T variation with respect to silicon thickness and oxide thickness is greater for DGJLT compared to DGMOS. The variation of V_T with respect to physical channel length is comparatively lesser in DGJLT than DGMOS. The SS variation with respect to L, T_{si} and T_{ox} were almost similar for both devices. In summary, DGJLT electrical parameters were more immune to channel length variations, while DGMOS were immune to T_{si} and T_{ox} variations.

Temperature dependence of the electrical characteristics of an n-type DGJLT is investigated. I_{ON} increases negligibly with increase in temperature for DGJLT; in contrast it follows the opposite trend in DGMOS. Drain current with respect to drain voltage increases with increase in increase in temperature, following the opposite trend in DGMOS. Intrinsic gain decreases with respect to T for DGMOS; however, for DGJLT, G_mR_O is almost independent of temperature after a gate voltage of ~ 0.6 V. The trend of f_T change with temperature is same for both the devices.

Chapter 4

Impact of Active Well Biasing on Process-Induced Variations of a Bulk Planer Junctionless Transistor

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In this work, the impact of process parameters namely gate length (L), thickness of silicon film (Tsi) and gate oxide thickness (Tox) with increased well bias on the electrical parameters viz., drain current (I_D), threshold voltage (V_T), subthreshold slope (SS) and drain induced barrier lowering (DIBL) of a short-channel bulk planer junctionless transistor (BPJLT) are systematically investigated with the help of extensive device simulations. The effect of positive well bias is utilized to improve the hot carrier effect of a BPJLT. The effect of well doping concentration on threshold voltage is studied. The threshold voltage variations with respect to well bias for different temperatures are studied.

There are many reports on the effects of well bias (V_W) on the performances and reliability of a single/multi-gate conventional MOSFET [56–66]. It is reported that active-well biasing can control its dynamic threshold voltage; forward well-biasing also helps in extending scalability of bulk-silicon technology; and improves hot-carrier reliability. Also, sensitivity of hot-carrier reliability is dependant of gate length

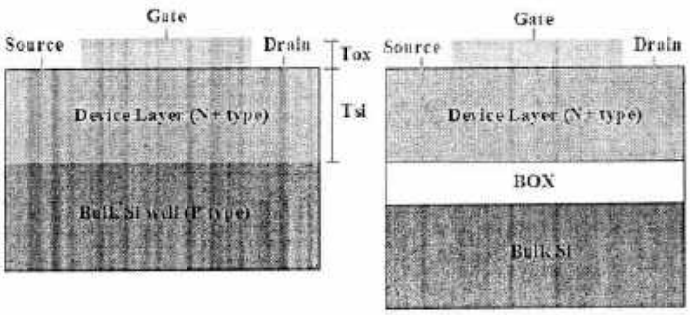

Figure 1: Cross-sectional view of (a) bulk planar junctionless transistor (BPJLT) (b) SOI Junctionless transistor (SOI-JLT).

for a given technology and body-bias factor. However, there is no systematic report on the effects of well bias on process parameters and hot-carrier reliability of a JLT to best of our knowledge. Here, effects of well bias on device performance parameters, namely, threshold voltage (V_T), SS, DIBL for varying channel length (L), silicon thickness (T_{si}) and gate-oxide thickness (T_{ox}) are studied for a shorter-channel length bulk-planer JLT with extensive device simulations using Silvaco TCAD simulations [48].

4.1 Device Structure And Simulation Setup

The device structure of the bulk planer junctionless transistor along with its SOI counterpart i.e., SOI-JLT are shown in Fig. 1. The working of the devices is explained in [14]. Device layer doping concentration (N_D) of 1.5×10^{19} cm^{-3}, well doping concentration (N_W) of 1×10^{16}–5×10^{18} cm^{-3}, equivalent gate oxide thickness (EOT)=1–2 nm, T_{si}=6–12 nm, L=10–50 nm and source/drain extension length (L_S/L_D)=20 nm are considered for TCAD simulations. Lombardi mobility model accounting for the dependence on the impurity concentrations as well as the transverse and longitudinal electric field values, Shockley-Read-Hall (SRH) recombination model to account for leakage currents, Fermi-Dirac carrier statistics without impact ionization, Band gap narrowing model (BGN) to take care of the band gap narrowing effect are used for simulations. Quantum effect is not considered except through the substrate-drain region. The transfer characteristic is calibrated with [14].

4.2 Simulation Results

It is reported that bulk planer JLT shows higher ON/OFF-state current ratio and better short-channel characteristics than

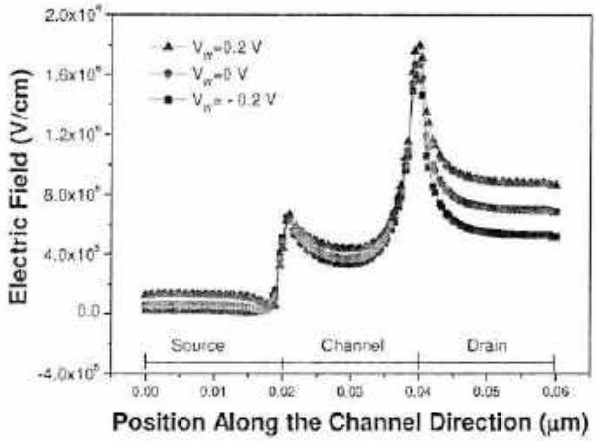

Figure 2: Electric field along the channel direction near the silicon-oxide interface for different well bias at V_{DS}=1 V, L=20 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

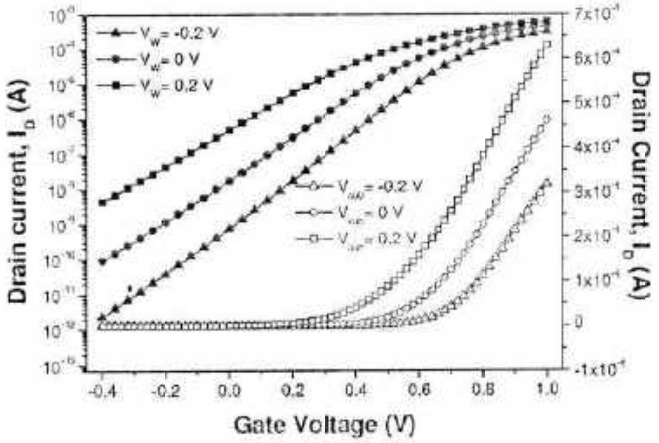

Figure 3: Transfer characteristics both in linear (right y-axis) and log (left x-axis) axis for different well bias at V_{DS}=1 V, L=20 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

a similar dimension SOI version of the JLT (SOI-JLT) [14].

The reason they claimed is that in bulk planer JLT, channel-well junction produces an additional depletion region which reduces the "effective channel thickness" improving the controllability of the gate and can be explained as follows. In a BPJLT, with no applied bias, the device layer is depleted from both top (because of its work function difference with the gate electrode and device layer) and bottom (device layer-well). The section of the physical device layer that is depleted by the gate at zero bias is the "effective device layer". When a positive bias is applied to the gate, this effective device layer comes out of depletion and results in a conducting channel between the source and the drain.

Thus, in the OFF-state, the device layers are depleted from both top and bottom of the channel region of the device. In the ON-state, however, a fraction of the device layer at the top—corresponding to the effective device layer—is in flatband, and the rest of it still remains depleted. Thus, a continuous conduction channel is formed in the ON-state, of which thickness is equal to the effective device layer thickness. In

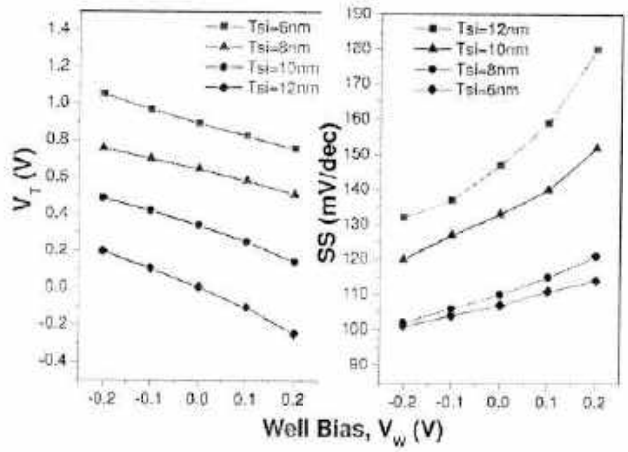

Figure 4: Variation of threshold voltage (at V_{DS}=1 V) and subthreshold slope with well bias for different substrate thickness. L=20 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

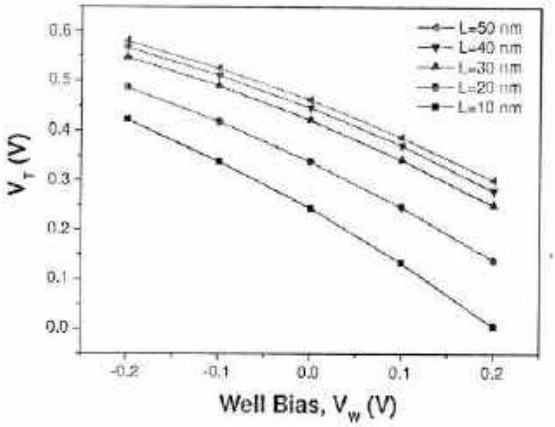

Figure 5: Variation of threshold voltage at a drain voltage of 1 V with well bias for L=10-50 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

case of SOI-JLT, the whole channel region is in the flatband region in the ON-state. Thus, for a JLT effective device layer thickness is thinner than physical thickness. The thinner effective device layer in the case of the BPJLT suggests that the device layer would be more controlled by the gate and consequently it would exhibit better electrostatic integrity than SOI-JLT. Also, it exhibits better I_{ON}/I_{OFF} than SOI-JLT.

Now with increased well bias, the effective device layer thickness increases for a JLT resulting in a decrease of controllability of the gate on the whole channel region and hence subthreshold characteristics are degraded. Thus, OFF-state current increases with increase in well bias. As a

consequence, with increased well bias, the threshold voltage decreases. A JLT has high vertical electric field in the OFF-state and near zero (i.e. flatband) electric field in the ON- state [29]. Thus, with increased well bias which results in more reduction in depletion region, I_{ON}.

As shown in Fig. 2, with increased well bias towards positive value, the electric field is decreased in the drain side, resulting in lowering of hot carrier effect for aforementioned

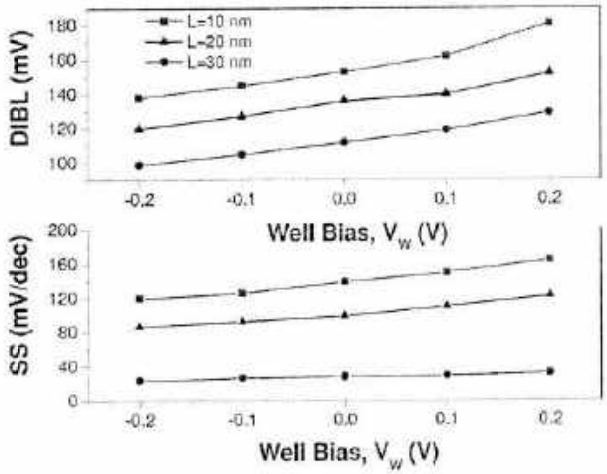

Figure 6: Subthreshold slope and drain induced barrier lowering with well bias for different channel length, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

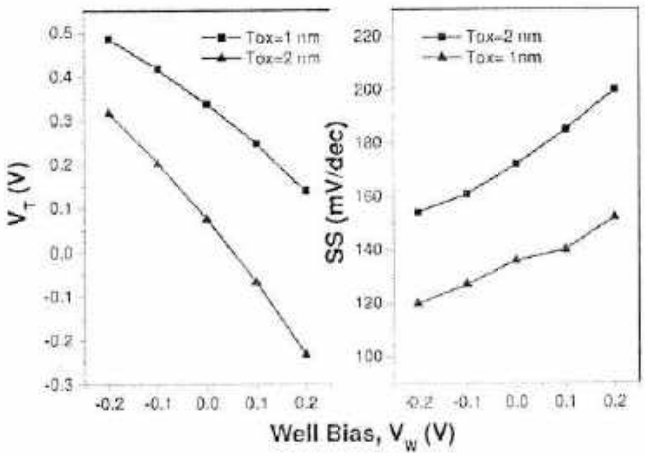

Figure 7: Variation of threshold voltage (at V_{DS}=1 V) and subthreshold slope with well bias for different gate oxide thickness. L=20 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

reason. The transfer characteristic of the device with increased well bias is shown in Fig. 3. As can be seen, though the ON-state current is improved slightly for higher V_W, OFF-state current is degraded making degradation of I_{ON}/I_{OFF}.

In a conventional MOSFET, the depletion charges remain mostly around source-channel-drain interface; however, for a JLT in the OFF-state whole of the substrate region is depleted of carriers. Unlike conventional MOSFET, where threshold voltage is dependent on the pn junction voltage, here in junctionless transistor it is determined by the amount of depletion charges. There is more threshold voltage variation with silicon layer thickness of a junctionless transistor compared to an inversion mode transistor due to more channel doping concentration for the former device [68–69]. However, there is less variation in the threshold voltage in junctionless transistor with an increase in channel length for the same substrate thickness for reason mentioned above. Fig. 4 shows the variation of threshold voltage (at V_{DS}=1 V) and subthreshold slope with well bias for different substrate

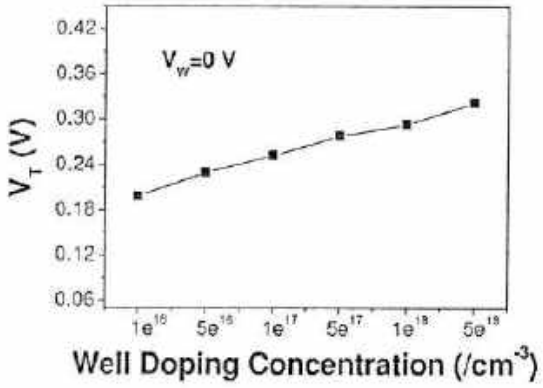

Figure 8: Variation of threshold voltage (at V_{DS}=1 V) with well doping concentration for different channel doping concentration. L=20 nm, Tsi=10 nm, Tox=1 nm. N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}, V_W=0 V

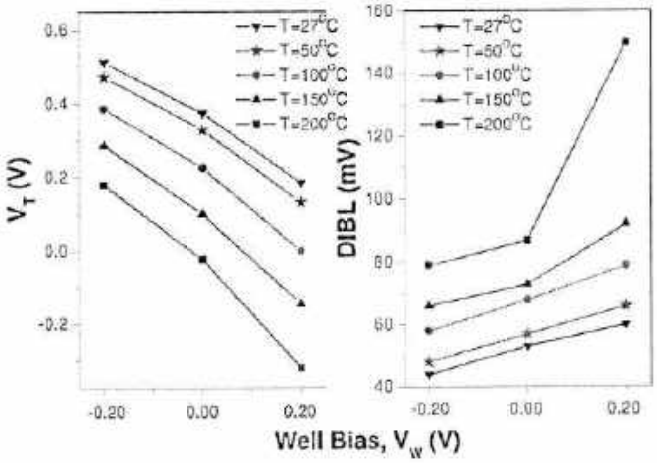

Figure 9: Variation of threshold voltage (at V_{DS}=1 V) and DIBL with well bias for temperatures T=27°C–200°C. L=20 nm, Tsi=10 nm, Tox=1 nm, N_D=1.5×10^{19} cm^{-3}, N_W=5×10^{18} cm^{-3}.

thickness. With an increase in well bias, threshold voltage decreases because of decrease in depletion region thickness. The variability increases slightly with an increase in channel doping concentration. With increase in the well bias which results in an increase in the effective device layer thickness, the gate controllability decreases, resulting in an increase of subthreshold slope; and this effect is more intense for increased substrate thickness.

With increased well bias, V_T decreases for different values of L; however, the rate of decrease is slightly higher for reduced L as seen in Fig. 5. Presented in Fig. 6, SS and DIBL increases slightly with well bias with the same trend for different L values. I_{ON}/I_{OFF} decreases slightly with positive values of well bias. These trends of changing V_T, SS and DIBL is similar for different values of T_{si} and T_{ox} [Fig. 7] as well. Well doping concentration also takes an important role in the device variability of the BPJLT. With increase in the well doping concentration, the workfunction difference between substrate region and p-type well region increases resulting in increase of depleted charges and hence threshold voltage as can be seen Fig. 8. This results in improvement of OFF-state current. However, with increase in well doping concentration, I_{ON} degrades because of effective flatband region in the channel region in the ON-state for reasons mentioned above.

In a conventional MOSFET, the decrease of threshold voltage with temperature tends to increase the drain current, while the reduction of mobility due to phonon scattering with temperature tends to decrease it [70]. However, in junctionless transistors, the reduction of mobility with temperature is much lower because of the bulk conduction mechanism [33, 35]. As a result, current increases in a monotonous manner with increase in temperature. This makes junctionless transistor favourable for high temperature applications. However, junctionless transistor has high threshold voltage variation

with temperature compared to conventional and accumulation-mode MOSFET because of high channel doping concentration. So, there is a reliability issue of high temperature applications of junctionless transistor. Thus, junctionless transistor can be used for high temperature applications where SiC is generally used, provided threshold variation lies within the tolerance limit. However, high quality defect and dislocation free SiC substrate are difficult to get and costly [71–73]. With an increase in well bias, the rate of decrease in threshold voltage with temperature increases as shown in Fig. 9. With an increase in well bias, threshold voltage decreases for any temperature. The decrease is more prominent for higher temperature. Well bias can be utilized to have a desired value of the threshold voltage at a given temperature. DIBL degrades for higher temperature; and it is worst for higher values of well bias.

4.3 Conclusion

The effects of well bias are utilized to improve the hot carrier effect of a bulk planer junctionless transistor. The effects of well bias on the device performance parameters, namely threshold voltage, drain current, SS, DIBL are studied. Though positive well bias helps in improving hot carrier effect; V_T decreases and SS, DIBL increases with forward V_W for different values of L, Tsi, Tox with almost similar trend. The change in threshold voltage with respect to the well doping concentration and well bias will affect circuit design reliability. Well doping concentration helps in improving the OFF-state current of the device at the cost of slight ON-state current degradation which however increases I_{ON}/I_{OFF} ratio. There is more V_T decrease with an increase in well bias for higher temperature. Well bias thus can be used to set the threshold voltage at any desired value.

Chapter 5

Channel Potential and Drain Current models for shorter-channel length DGJLT

5.1 Introduction

Looking at the low leakage currents and other advantages as mentioned in previous chapters, a JLT can be adjusted as a prospective candidate for low power circuit design applications in future technology nodes, and therefore, an analytical compact model of junctionless transistor is sought after. Since the device physics of DGJLT is fundamentally different than the JB MOSFETs, the existing models for DG JB MOSFETs do not directly apply. There are many reports on analytical/semi-analytical modelling for potential and drain current either for long-channel or short-channel length junctionless transistor in double-gate, trigate and gate-all-around architecture till date [44, 46, 74, 75-76, 77, 78, 79-90]. Some of them are valid only in subthreshold region and some are applicable from subthreshold to accumulation region. Also, some of the models are developed piecewise (region-wise) and some are non-piecewise. Gnani et al. reported a charge based cylindrical model for JLT [63]. Chen et al. reported a surface potential based piecewise model for drain current for long channel DGJLT [77]. Sallese et al. demonstrated a charge based model for drain current for long channel DGJLT [74], which may cause some convergence problem as indicated by [77]. Lime et al. demonstrated a charge based simple compact model for drain current of DGJLT [79]. Duarte et al. proposed a nonpiecewise full-range drain current model for long-channel DGJLT [76]. They also proposed an analytical bulk current model using the depletion width concept for long channel DGJLT [46], but neglected the accumulation region. They also have reported a compact model of quantum electron density at the subthreshold region for DGJLT [80]. They also proposed a nonpiecewise model for long channel junctionless cylindrical nanowire FETs [81]. Chiang derived a quasi-2D threshold voltage model for short-channel DGJLT [78]. Gnudi et al. proposed a semianalytical model of the subthreshold current of DGJLT [97]. Trevisoli et al. derived a physically-based threshold voltage definition and extraction method for trigate JLT [82]. Trevisoli et al. also reported threshold voltage model for JLT with cylindrical and rectangular geometries [83]. Trevisoli et al. proposed a drain current model accounting short-channel-effects for a p-type gate-all-around JLT [84]. Gnudi et

al. proposed an analytical model for threshold voltage variability due to random dopant fluctuations in junctionless FETs [44]. Cerdeira et al. reported a charge based continuous model for long channel DGJLT [91]. They also demonstrated an empirical potential model for long channel DGJLT [85]. Variable separation technique was used for potential and drain current modeling of DGJLT for short channel-lengths which was valid in subthreshold region [95]. Yesayan et al. proposed an explicit drain current model for long channel DGJLT using charge based method [86]. Hu et al. proposed an analytical model for electric potential, threshold voltage and subthreshold swing of short-channel junctionless surrounding-gate MOSFETs [87]. Woo et al. proposed an analytical threshold voltage model of junctionless DGJLT with localized charges [88]. Li et al. proposed the subthreshold behaviour models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs [89]. Trevisoli et al. proposed a surface potential based drain current analytical model for short-channel trigate junctionless nanowire transistors valid in subthreshold region [90]. There are few potential models for shorter channel length double-gate junctionless transistors which are valid in subthreshold region only. Jiang et al. proposed a physics-based analytical model of electrostatic potential for short-channel junctionless double-gate MOSFETs (JLDGMTs) operated in the subthreshold regime only by solving 2D Poisson's equation in channel region by a method of series expansion similar to Green's function [98]. Jin et al. derived potential model by solving 2-D Poisson's equation using "variable separation technique" for deep nanoscale short channel asymmetric junctionless Double-Gate (DG) MOSFETs valid in the subthreshold region [99]. Holtij et al. reported analytical 2D potential model within ultra-scaled junctionless double-gate MOSFETs (DG MOSFETs) valid in the subthreshold regime using the Schwarz-Christoffel transformation [100]. Accurate potential and drain current models, valid from depletion to accumulation regions of operation, for shorter channel length double-gate junctionless transistor, are still rare in literature.

5.2 A Surface Potential based Drain Current model for Short-Channel Junctionless Double-Gate MOSFETs (DGJLT)

In this work, potential and drain current models, covering all regions of operation, are targeted for a shorter channel length double-gate junctionless transistor (DGJLT). A two-part approach, known as the "variable separation technique" is applied to derive the channel potential, in which the total potential is divided into long channel part and short channel part. Such a method gives quite accurate results in short channel regime, because, while deriving the short channel part of potential, one can include a large set of eigenvalues and details will be presented in later section. Threshold voltage and drain induced barrier lowering (DIBL) parameters are e xtracted from the model. The potential model as well as the extracted parameters is then

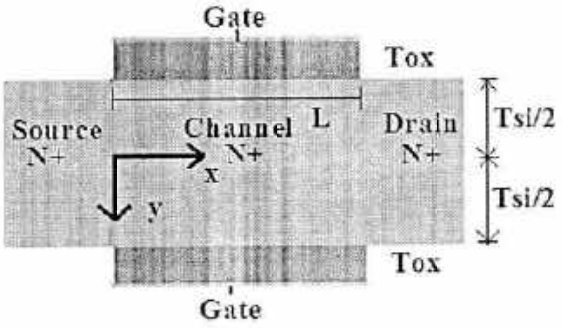

Figure 5.1: Cross-sectional view of symmetric n-channel double-gate junctionless transistor (DGJLT) with channel direction.

compared to professional TCAD simulation results.

5.2.1 Model Derivation

The Poisson's equation considering both fixed and mobile charges in the silicon region can be written as

$$\frac{d^2\Psi(x,y)}{dx^2}+\frac{d^2\Psi(x,y)}{dy^2}=\frac{qN_D}{\varepsilon_{si}}\left(e^{(\Psi(x,y)-V)/U_T}-1\right) \tag{5.1}$$

Where, $\Psi(x,y)$ is the channel potential. ε_{si} is the permittivity of silicon. V is electron quasi-Fermi potential, U_T=kT/q is the thermal voltage, N_D is the channel doping concentration and q is the charge of electron. Hole density is neglected as compared to electron density. The coordinates, x and y are as shown in Fig 5.1. Equation (5.1) has no direct analytical solution. One way to solve (5.1) is variable separation technique, which states that the total potential can be divided into long channel part (1D) and short channel part (2D) i.e,

$$\Psi(x,y)=\Psi_I(y)+\Psi_{II}(x,y) \tag{5.2}$$

Where, $\Psi_I(y)$ is the potential which is related to only y direction (long channel part) and $\Psi_{II}(x,y)$ is related to both x and y direction of the potential variation (short channel part) with below stated boundary conditions.

Expression for $\Psi_I(y)$:

$\Psi_I(y)$ is expressed as

$$\frac{d^2\Psi_I}{dy^2}=\frac{qN_D}{\varepsilon_{si}}\left(e^{(\Psi_I(y)-V)/U_T}-1\right) \tag{5.3}$$

with boundary conditions

$$\left.\frac{\partial\Psi}{\partial y}\right|_{y=\pm\frac{T_{si}}{2}} = \Psi_S = \frac{C_{ox}}{\varepsilon_{si}}\left(V_{GS} - V_{FB} - \Psi\left(\frac{T_{si}}{2}\right)\right)$$
$$\left.\frac{\partial\Psi}{\partial y}\right|_{y=0} = 0 \tag{5.4}$$

Equation (5.4) has no closed form solution even though it looks simple. Integrating (5.4), we obtain

$$E_S^2 = \frac{2qN_D U_T}{\varepsilon_{si}}\left[e^{(\Psi_S - V)/U_T} - e^{(\Psi_0 - V)/U_T} - \left(\frac{\Psi_S - \Psi_0}{U_T}\right)\right] \tag{5.5}$$

Where, Ψ_S and Ψ_0 are the potential at the surface and centre of the channel respectively. Thus, once the relation between Ψ_S and Ψ_0 is known, the potential at any point in the silicon body can be determined. The Gauss's law connects the surface potential with gate voltage as

$$Q_{SC} = -2\varepsilon_{si}\left.\frac{d\Psi}{dx}\right|_{x=\pm\frac{T_{si}}{2}} = -2C_{ox}(V_G - V_{FB} - \Psi_S) \tag{5.6}$$

Q_{SC} being the space charge density per unit area, $C_{ox} = \varepsilon_{ox}/T_{ox}$ is the oxide capacitance, V_{FB} is the flat band voltage. Combining (5.5) and (5.6)

$$(V_G - V_{FB} - \Psi_S)^2 = \frac{2qN_D\varepsilon_{si}U_T}{C_{ox}^2}\left[e^{(\Psi_S - V)/U_T} - e^{(\Psi_0 - V)/U_T} - \left(\frac{\Psi_S - \Psi_0}{U_T}\right)\right] \tag{5.7}$$

a) For depletion region $(V_{FB} < V_G < V_{FB} + V_{DS})$ *with* $V_{DS} > 0$, the equation (5.7) after some mathematical reformations can be written as [67]

$$\Psi_S = V_G - V_{TH} - \frac{qN_D T_{si}}{8C_{si}} - V_T\, Lambertw\left[\frac{qN_D T_{si}}{4C_{ox}U_T}e^{(V_G - V_{TH} - V)/U_T}\right] \tag{5.8}$$

Where, Lambertw is the Lambert W-function, which is the inverse of the function $z = W(z)e^{W(z)}$. V_T is the threshold voltage and $(\Psi_0 - \Psi_S)$ is the difference of centre and surface potential given by,

$$V_T = V_{FB} - qN_D T_{si}/2C_{eff}$$
$$C_{eff}^{-1} = (4C_{si})^{-1} + (C_{ox})^{-1},\quad C_{si} = \varepsilon_{si}/T_{si} \tag{5.9}$$
$$\Psi_0 - \Psi_S = qN_D T_{si}^2/8\varepsilon_{si}$$

The expression of V_T in (5.9) is valid when channel length is higher. The V_T for shorter-channel device is given later section.

b) For accumulation region $(V_G > V_{FB} + V_{DS})$

The relation between centre and surface potential $\{\Psi_S - \Psi_0 (= \alpha, \text{say})\}$ is given by [48]

$$\Psi_S - \Psi_0 = \frac{qN_D T_{si}^2}{8\varepsilon_{si}}\left(e^{\frac{\Psi_0 - V}{U_T}} - 1\right) \tag{5.10}$$

Equation (5.10) can also be expressed as [91]

$$\Psi_s - \Psi_0 = -\frac{qN_D T_{si}}{8C_{si}} + U_T Lambertw\left[\frac{qN_D T_{si}}{8C_{si}U_T} e^{\frac{qN_D T_{si}}{8C_{si}U_T}} e^{\frac{\Psi_s - V}{U_T}}\right] \tag{5.11}$$

Now, using (5.7) and (5.11), the relation between surface potential with gate voltage can be obtained as [65]

$$\begin{aligned}(V_G - V_{FB} - \Psi_s)^2 = sign(\alpha)\left(\frac{q^2 N_D{}^2 T_{si}^3 \varepsilon_{si}}{C_{ox}{}^3}\right)\left[e^{(\Psi_s - V)/U_T} - 1 - \left(1 + \frac{8C_{si}U_T}{qN_D T_{si}}\right)\right. \\ \left.\times\left\{-\frac{qN_D T_{si}}{8C_{si}U_T} + Lambertw\left[\frac{qN_D T_{si}}{8C_{si}U_T} e^{\frac{qN_D T_{si}}{8C_{si}U_T}} e^{\frac{\Psi_s - V}{U_T}}\right]\right\}\right]\end{aligned} \tag{5.12}$$

For accumulation region ($V_{GS} > V_{FB} + V_D$), $\alpha > 0$. Equation (5.12) can only be solved numerically. The centre potential can be derived using equations (5.8) – (5.12), also explained in [85].

Expression for $\Psi_{II}(x, y)$:

$\Psi_{II}(x, y)$ is expressed as

$$\frac{d^2\Psi_{II}(x, y)}{dx^2} + \frac{d^2\Psi_{II}(x, y)}{dy^2} = 0 \tag{5.13}$$

with the boundary conditions

$$\begin{aligned}&\Psi_{II}(0, y) = V_{bi} - \Psi_s(y) \\ &\Psi_{II}(L, y) = V_{DS} + V_{bi} - \Psi_s(y) \\ &\varepsilon_{si}\frac{\partial\Psi_{II}(T_{si}/2, x)}{\partial x} = -C_{ox}\Psi_{II}\left(\frac{T_{si}}{2}, x\right) \\ &\left.\frac{\partial\Psi_{II}}{\partial y}\right|_{y=0} = 0\end{aligned} \tag{5.14}$$

Equation (5.13) is a mixed boundary value problem and it is already solved by many groups [101]-[102]. The final solution is

$$\Psi_{II}(x, y) = \left\{A_0 e^{\frac{2\mu_n(x-L)}{T_{si}}} + A_1 e^{-\frac{2\mu_n x}{T_{si}}}\right\} \times \cos(\mu_n y) \tag{5.15}$$

Where,

$$\begin{aligned}A_0 &= B_1\left[V_{DS} + V_{bi}\left(1 - e^{-\frac{2\mu_n L}{T_{si}}}\right)\right] - B_2\Psi_{S(Lang)} \\ A_1 &= B_1\left[V_{bi}\left(1 - e^{-\frac{2\mu_n L}{T_{si}}}\right) - V_{DS}e^{-\frac{2\mu_n L}{T_{si}}}\right] - B_2\Psi_{S(Lang)}\end{aligned} \tag{5.16}$$

$$B_1 = \frac{4\times Sin(\mu_n)}{2\mu_n + Sin(2\mu_n)\left(1-e^{-\frac{2\mu_n L}{T_{si}}}\right)},\quad B_2 = \frac{4\mu_n \times Cos\left(\frac{\mu_n}{2}\right)\left(1-e^{-\frac{2\mu_n L}{T_{si}}}\right)}{2\mu_n + Sin(2\mu_n)\left(1-e^{-\frac{2\mu_n L}{T_{si}}}\right)} \tag{5.17}$$

$\Psi_{s(Long)}$ is the long channel surface potential. The eigen-value μ_n is the periodic n^{th} root of this equation and determined using the permittivity and thickness of both silicon and oxide. It can have infinite possible values for μ. However, first 1-2 iteration(s) give quite good result.

$$2\mu_n \tan(\mu_n) = \frac{\varepsilon_{ox} T_{si}}{T_{ox}\varepsilon_{si}} \tag{5.18}$$

Now, putting the expressions of $\Psi_1(y)$ and $\Psi_n(x,y)$ in equation (5.2), the total potential in the channel region of a short channel DGJLT can be determined.

Threshold voltage extraction

A schematic plan for calculating the threshold voltage (V_T) is given in Fig. 5.2. The threshold voltage is given by the following expression, and it is valid for longer as well as shorter channel length devices [103]

$$V_T = V_{GS} + \Delta V_{GS}\left(\frac{U_T \ln(N_D/n_i) - \Psi_{min(V_{GS1})}}{\Psi_{min(V_{GS2})} - \Psi_{min(V_{GS1})}}\right) \tag{5.19}$$

$\Psi_{min(V_{GS2})}$ and $\Psi_{min(V_{GS1})}$ are the minimum potentials at two gate-to-source voltages V_{GS1} and V_{GS2}. Assuming a linear relationship between Ψ_{min} and V_{GS} in the subthreshold region, threshold voltage can be extracted using (13).

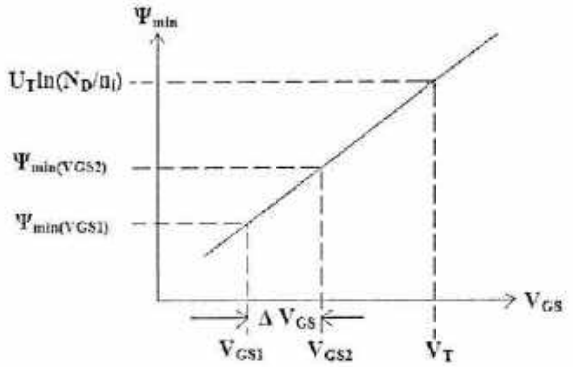

Figure 5.2: Schematic plan for calculating the threshold voltage. Here, $V_T = V_{GS}$ at $U_T\ln(N_D/n_i) = \Psi_{min}$. ΔV_{GS} is the difference between two voltages in the subthreshold region.

Drain induced barrier lowering (DIBL) is defined as the change in threshold voltage when drain voltage changes from 50 mV to 1 V i.e.,

$$DIBL = V_T\big|_{V_{DS}=50mV} - V_T\big|_{V_{DS}=1V} \tag{5.20}$$

5.2.2 Discussion and Verification of Model

To validate the model results, they are compared with electrical characteristics for the devices simulated using 2D ATLAS device simulator with version 5.19.20.R [48]. Lombardi mobility model is employed, accounting for the dependence on the impurity concentrations as well as the transverse and longitudinal electric field values. Shockley-Read-Hall (SRH) recombination model is included in the simulation to account for leakage currents. Because of high channel doping concentration, Fermi-Dirac carrier statistics without impact ionization is utilized in the simulations. Band gap narrowing model (BGN) is also incorporated to take care of the band gap narrowing effect which may arise due to highly doped channel regions. Quantum effect is not considered here. Channel doping concentration N_D of 5×10^{18} and 1×10^{19} cm^{-3}, equivalent gate oxide thickness (EOT) = 2 nm, silicon thickness (T_{si}) = 10, 15 nm are considered for TCAD simulation. Channel width (W) is 1μm. In addition, p-type polysilicon is used having doping concentration 10^{20} cm^{-3}. The interface charge concentration (N_{SS}) is considered as 5×10^{10} cm^{-3}. A constant mobility (μ_0) of 100 $cm^2/V.s$ is assumed.

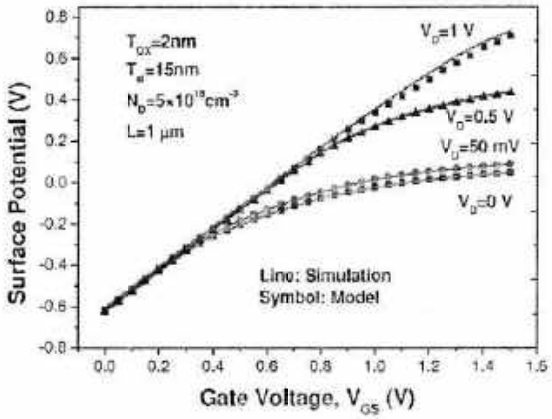

Figure 5.3: Surface potential with respect to gate voltage near the drain side for V_D=0 V, 50 mV, 0.5 V and 1 V. L=1 μm, T_G=15 nm, T_{OX}=2 nm, $N_D=5\times10^{18}$ cm^{-3} and source/drain extension length=50 nm. Flat band voltage (V_{FB}) is considered as ~1.1 eV.

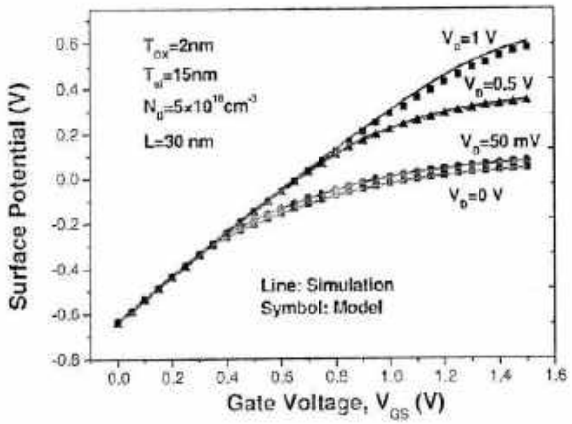

Figure 5.4: Surface potential with respect to gate voltage near the drain side for V_D=0 V, 50 mV, 0.5 V and 1 V. L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D=5×10^{18} cm^{-3} and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as ~1.1 eV.

For channel length of 1 μm, source/drain extension length (L_S/L_D) is taken as 50 nm; and for channel length of 30 nm-80 nm, L_S/L_D is taken as 10 nm to avoid parasitic resistance effect. Calculations are done on Mathematica computational software. Fig. 5.3 shows the surface potential with respect to gate voltage, for different values of V_D=0 V, 50 mV, 0.5 V and 1 V respectively for channel length of 1 μm. The simulation and model curves are in close agreement. Fig. 5.4 shows the surface potential with respect to gate voltage, for different values of V_D=0 V, 50 mV, 0.5 V and 1 V respectively for channel length of 30 nm. The marginal difference may be due to the inclusion of source and drain

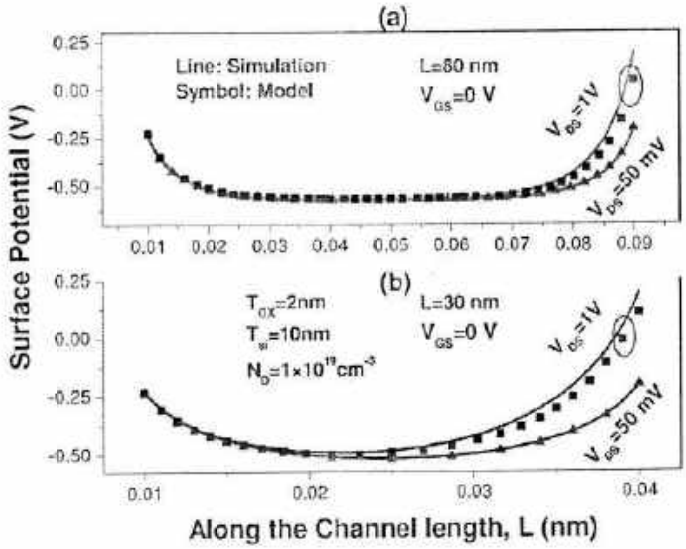

Figure 5.5: Surface potential along the channel for (a) L=80 nm (long channel) at V_D=50 mV, 1V (b) L=30 nm (short channel). T_{si}=10 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3}, V_{GS}=0 V and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as ~1.1 eV.

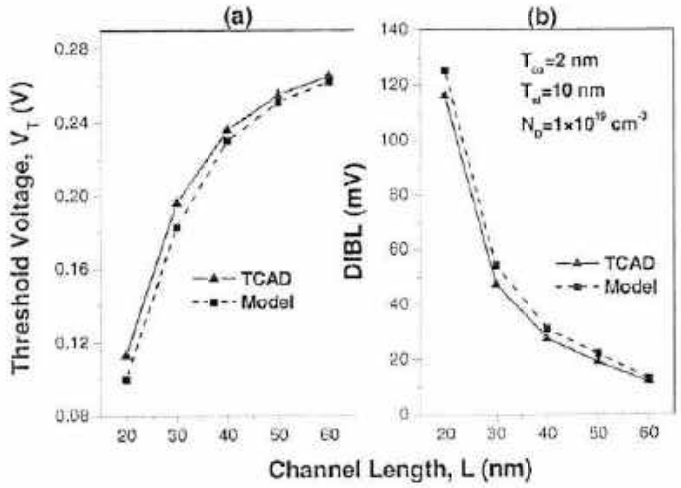

Figure 5.6: (a) Threshold voltage (V_T) at V_{DS}=50 mV for L=20 nm to 60 nm (b) drain induced barrier lowering (DIBL) for L=20 nm to 60 nm. T_{si}=10 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3}.

extension resistances in TCAD characteristics; and the exclusion of fringing electric fields and quantum effects in the model. Fig. 5.5 (a) and (b) shows the potential along the channel direction, 0.5 nm away from the Si-SiO_2 interface, at V_{DS} = 50 mV and 1 V respectively keeping V_{GS}=0 V at gate length of 80 nm and 30 nm. Both the simulation and model plots are in close agreement. There is marginal difference of potential towards the drain side between model and simulation. For example, for L = 30 nm at VDS = 1 V this difference are 86.4 mV. Fig. 5.6 (a) and (b) shows the threshold voltage and drain induced barrier lowering characteristics extracted from model and simulation, for different gate lengths. The values obtained from model and simulation are in close agreement. The marginal difference of threshold voltage between model and TCAD results for say, L=20 nm and L=60 nm are 0.013 and 0.003 V respectively. The difference of DIBL between model and TCAD results are 9 mV and 1 mV for L = 20 nm and L = 60 nm respectively.

5.2.3 Drain Current Model

The mobile charge density Q_m can be written as

$$Q_m = Q_{SC} - Q_d \tag{5.21}$$

$Q_d = qN_D T_{si}$ is the fixed charge density. The drain current can be expressed as (using (5.7))

$$I_D = -\mu \frac{W}{L} \int_0^{V_{DS}} Q_n dV$$
$$= -\mu \frac{W}{L} \int_0^{V_{DS}} \left[2C_{ox} \left(V_G - V_{FB} - \Psi_S \right) + Q_d \right] dV \tag{5.22}$$

It is assumed that V_S=0 and V_D=V_{DS}. W is the width of the device and Ψ_S (long-channel part + short-channel part) is the surface potential. Fig. 5.6 shows the drain current with respect to gate voltage for different values of N_D i.e., 8×10^{18} cm^{-3} and 1×10^{19} cm^{-3} at a drain voltage of 1 V. Same current values are plotted in both logarithmic (left) and linear scales (right). The model results (symbols) are in

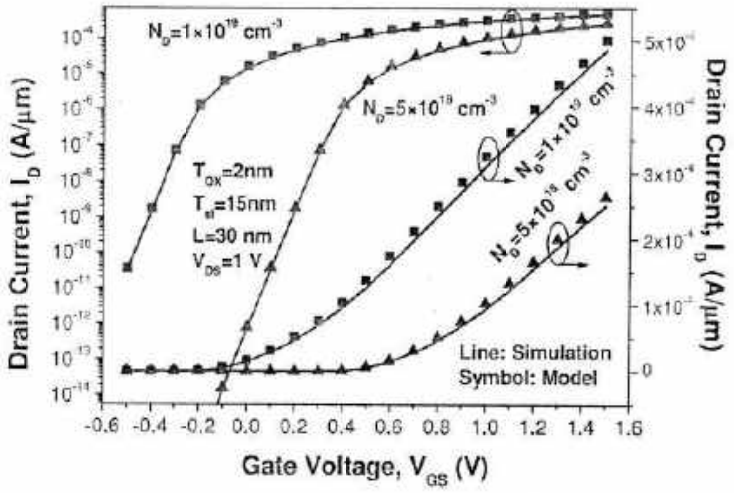

Figure 5.7: Drain current with respect to gate voltage for N_D=5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}. L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, V_{DS}=1 V and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as ~1.1 eV. Lines show the TCAD simulations and symbols shows model results.

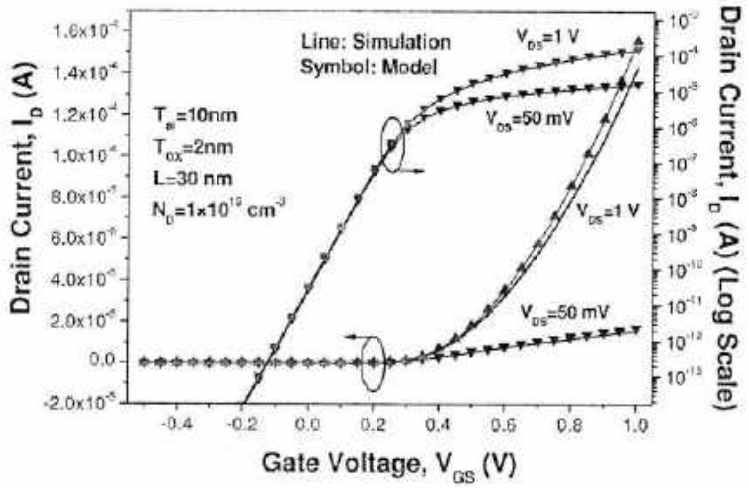

Figure 5.8: Drain current with respect to gate voltage for T_{si}=10 nm, L=30 nm, T_{ox}=2 nm N_D= 1×10^{19} cm^{-3} and source/drain extension length=10 nm at V_{DS}=50 mV and 1 V. Lines show the TCAD simulations and symbols show model results.

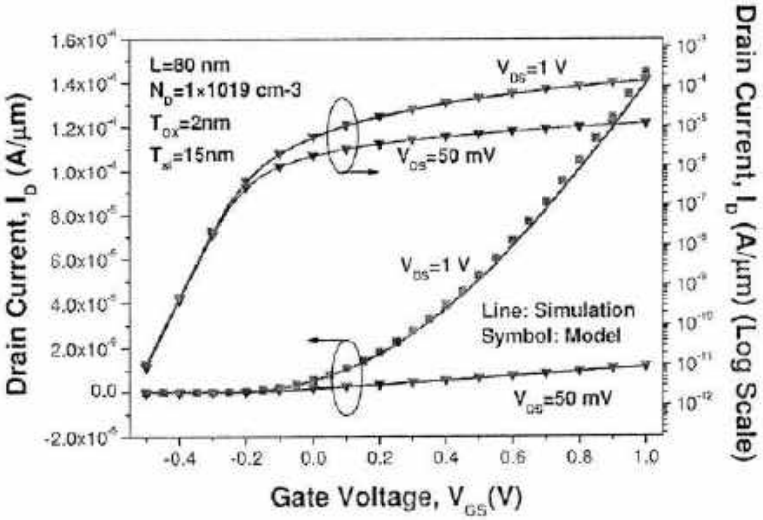

Figure 5.9: Drain current with respect to gate voltage for L=80 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D= 1×10^{19} cm^{-3} and source/drain extension length=10 nm at V_{DS}=50 mV and 1 V. Lines show the TCAD simulations and symbols show model results.

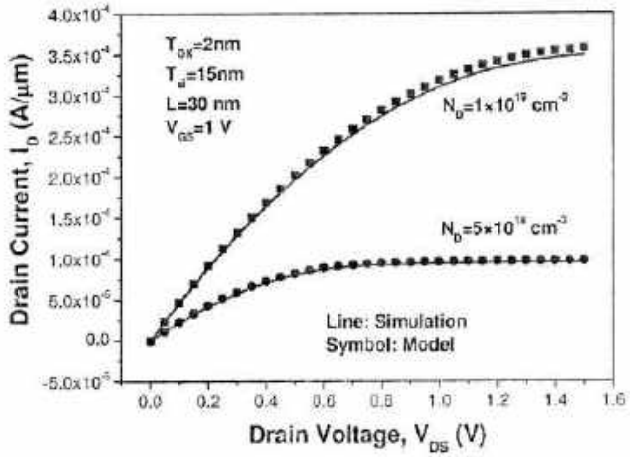

Figure 5.10: Drain current with respect to drain voltage for N_D=5×10^{18} cm^{-3} and 1×10^{19} cm^{-3}. L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, V_{GS}=1 V and source/drain extension length=10 nm. Flat band voltage (V_{FB}) is considered as -1.1 eV. Lines show the TCAD simulations and symbols shows model results.

close agreement with TCAD simulation (lines) in all regions of device operation, i.e., subthreshold to accumulation region. The subthreshold slope obtained from model is almost equal to TCAD results.

As expected, current saturates at higher gate voltage. Also, saturation current increases with increase in channel doping concentration as usual. The current in the accumulation region is obtained numerically. The subthreshold slope extracted from model and TCAD are in close agreement for long as well as short channel DGJLT. For example, for a DGJLT with L=30nm, T_{si}=10 nm, T_{ox}=2 nm and N_D=1×10^{19} cm^{-3}, the subthreshold slope is 63 mV/dec as extracted from TCAD, which is almost similar to the value extracted from model. Fig. 5.8 shows the transfer characteristic for Tsi=10 nm, L=30nm, T_{ox}=2 nm and N_D=1×10^{19} cm^{-3} at gate voltages V_{GS} of 50 mV and 1 V. Both TCAD (solid line) and model results (symbols) are in close agreement. Fig. 5.9 shows the drain current with respect to gate voltage for L=80 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D= 1×10^{19} cm^{-3} at V_{DS}=1 V. Lines show the TCAD simulations and symbols shows model results. TCAD (solid line) and model results (symbols) are in good agreement. Fig. 5.10 presents the drain current with respect to drain voltage for different values of N_D i.e., 8×10^{18} cm^{-3} and 1×10^{19} cm^{-3} at a gate voltage of 1 V. The models (symbols) are in close accord with TCAD simulation (lines). The transconductance with respect to gate voltage for L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3} at V_{DS}=1 V is shown in Fig. 5.11. TCAD simulations (symbols) and model results (lines) are not in close match at higher gate voltages. Fig. 5.12 shows the output conductance with respect to drain voltage for L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3} at V_{GS}=1 V. Both TCAD and model results are in close agreement.

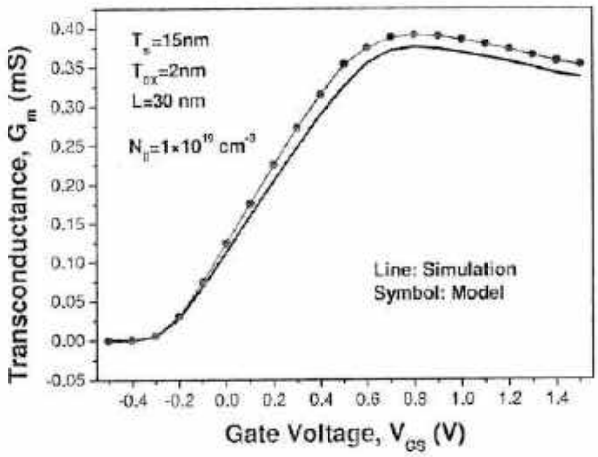

Figure 5.11: Transconductance with respect to gate voltage for L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3} at V_{DS}=1 V and source/drain extension length=10 nm. Lines show the TCAD simulations and symbols shows model results.

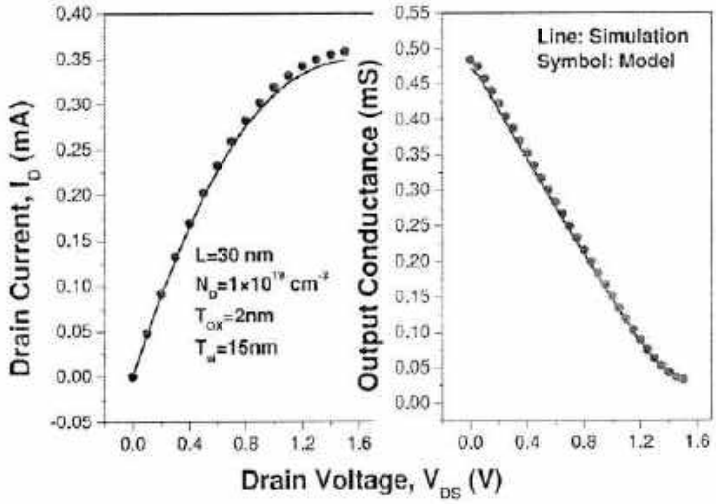

Figure 5.12: Drain current and output conductance with respect to drain voltage for L=30 nm, T_{si}=15 nm, T_{ox}=2 nm, N_D=1×10^{19} cm^{-3} at V_{GS}=1 V and source/drain extension length=10 nm. Lines show the TCAD simulations and symbols shows model results.

5.3 Summary

A semi-analytical model is proposed to calculate the channel surface potential as well as drain current for shorter channel length symmetric double-gate junctionless transistor with potential two parts approach. Carrier mobility is assumed constant. Quantum effects are not considered. The model is valid in depletion to accumulation region of operation. Threshold voltage and drain induced barrier lowering parameters were extracted from model. Assessment of the model with TCAD simulations confirms its legitimacy. Consideration of short-channel and quantum effects in the model is another scope for future research.

Chapter 6

Conclusions and Future Scope of the Work

9.1 Conclusion

Low power and high performance devices are in demand for today's microelectronics market. Recently, junctionless transistor has proven itself as a very promising device in this arena. The first part of the work discusses about the analog and digital performances; process and temperature effects of a double-gate junctionless transistor. In the second part, effects of well bias are utilized to improve the hot carrier effect of a bulk planer junctionless transistor. In the last part an analytical channel potential model for shorter-channel double gate junstionless transistor (DGJLT) is developed.

It is observed that

- Double-gate JLT show better device performance characteristics in terms of SCEs, G_m/I_D and intrinsic gain compared to its similar dimension IM counterpart and later device outperforms in terms of speed.
- DGJLT electrical parameters are more immune to channel length variations. However, there is a notable threshold voltage change of the device with silicon thickness compared to a JB device.
- Unlike JB MOSFET, overall performance of a DGJLT is not degraded much by increase in temperature and use of high-k gate dielectrics.
- The effects of well bias are utilized to improve the hot carrier effect of a bulk planer junctionless transistor. Though positive well bias helps in improving hot carrier effect; V_T decreases and SS, DIBL increases with forward V_W for different values of L, Tsi, Tox with almost similar trend. Well doping concentration helps in improving the OFF-state current of the device at the cost of slight ON-state current degradation which however increases I_{ON}/I_{OFF} ratio. There is more V_T decrease with an increase in well bias for higher temperature. Well bias thus can be used to set the threshold voltage at any desired value.

9.2 Future Scope of the Work

The findings presented in this work are mostly based on the simulation results including appropriate models. This helped us to arrive at a qualitative understanding of the device operation. More rigorous information can be obtained by full quantum simulations using either non-equilibrium green's function (NEGF) approach or Wigner-function approach. There is lot of scope for compact modelling for circuit simulation of shorter channel length JLT which includes all short channel effects like hot carrier effect, velocity saturation effect, drain induced barrier lowering effect etc and process induced variation parameters. Designing circuits including process induced variation parameters for low power applications is a fine scope of work. Also, implementation of the working models in spice simulator for circuit simulation is another scope for extending the work. Studying the reliability issues in DGJLT and developing compact models with reliability issues in the model is excellent scope of research.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits", Electronics, vol. 38, no. 8, 1965.

[2] International Technology Roadmap for Semiconductors (ITRS), 2001 edn. (http://www.itrs.net/).

[3] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros et al., "High performance fully-depleted tri-gate CMOS transistors", IEEE Electron Device Lett., vol. 2, pp. 263–265, 2003.

[4] P. J.-Tae, J. P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines", IEEE Trans. on Electron Devices, vol. 49, pp. 2222–2229, 2002.

[5] P. J.-Tae, J. P. Colinge, C. H. Diaz, "Pi-Gate SOI MOSFET", IEEE Electron Device Lett., vol. 22, pp. 405–406, 2001.

[6] J. T. Park, C. A. Colinge, J. P. Colinge, "Comparison of gate structures for short-channel SOI MOSFETs", IEEE International SOI Conference, pp. 115–116, 2001.

[7] Y. F.-Liang, C. H.-Yu, C. F.-Cheng, H. C.-Chuan, C. C.-Yun, C. H.-Kuang, et al., "25 nm CMOS Omega FETs", Electron Devices Meeting, IEDM '02 Technical Digest pp. 255–258, 2002.

[8] J. P. Colinge, M. H. Gao, A. R.-Rodriguez, H. Maes and C. Claeys, "Silicon-on-insulator gate-all-around device", International Electron Devices Meeting, IEDM '90 Technical Digest, pp. 595–598, 1990.

[9] R. Yu, "A study of silicon and germanium junctionless transistors", Ph.D Thesis, University College Cork, 2013.

[10] A. Kranti, C. W. Lee, I. Ferain, R. Yu, N. D. Akhavan, P. Razavi and J. P. Colinge, "Junctionless nanowire transistor: Properties and design guidelines", in Proc. IEEE 34th Eur. Solid- State Device Res. Conf., pp. 357–360, 2010.

[11] A. Amara, O. Rozeau, "Planar double-gate transistor: From technology to circuit", Springer, 2009.

[12] I. Ferain, C. A. Colinge and J.-P. Colinge, "Multigate transistors as the future of classical metal–oxide–semiconductor field-effect transistors, Nature, vol. 479, pp. 310-316, Nov. 2011.

[13] J.-P. Colinge, "FinFETs and other multi-gate transistors", Springer, 2008.

[14] A. M. Ionescu, H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches", Nature, vol. 479, pp. 329–337, Nov. 2011.

[15] K. Boucart, A. M. Ionescu, "Double-gate tunnel FET with high-κ gate dielectric", IEEE Trans. on Electron Devices, vol. 54, no. 7, pp. 1725–1733, July 2007.

[16] S. Mahapatra, A. M. Lonescu, "Hybrid CMOS single-electron-transistor device and circuit

design", Artech House, Sep. 2006.

[17] M. M. Shulaker, G. Hills, N. Patil, H. Wei, H.-Y. Chen, H.-S. P. Wong and S. Mitra, "Carbon nanotube computer", Nature, vol. 501, pp. 526–530. Sep. 2013.

[18] S. Reich, C. Thomsen and J. Maultzsch, "Carbon nanotubes: Basic concepts and physical properties", Wiley, 2004.

[19] B. Razavi, "Design of analog CMOS integrated circuits", Tata McGraw-Hill Edn. 2002.

[20] B. G. Streetman, S. Banerjee, "Solid state electronic devices", PHI 5th Edn., 2005.

[21] Y. Taur, T. H. Ning, "Fundamentals of Modern VLSI devices", Cambridge Univ. press, 1st Edn.

[22] D. A. Neamen, D. Biswas, "Semiconductor physics and devices", Tata McGraw-Hill 4th Edn.

[23] J. D. Plummer, M. D. Deal and P. B. Griffin, "Silicon VLSI technology: Fundamentals, practice and modeling", Pearson, 1st Edn.

[24] N. DasGupta, A. DasGupta, "Semiconductor devices: Modeling and technology", PHI, Oct. 2011.

[25] S.M. Sze, "VLSI Technology", Tata McGraw-Hill 2nd Edn., 2003.

[26] J. E. Lilienfield, "Method and apparatus for controlling electric currents", US patent, 1745175, 1925.

[27] J. E. Lilienfield, "Device for controlling electric current", US patent, 1900018, 1928.

[28] P. Mondal, B. Ghosh and P. Bal, "Planar junctionless transistor with non-uniform channel doping", Appilied Physics Lett., vol. 102, 133505, 2013.

[29] J. P. Colinge, C. W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A..M. Kelleher, B..McCarthy and Richard Murphy, "Nanowire transistors without junctions", Nat. Nanotechnol., vol. 5, no. 3, pp. 225–229. 2010.

[30] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain and J.-P. Colinge, "Junctionless multigate field- effect transistor", Appl. Phys. Lett., vol. 94, no. 5, pp. 053 511-1–053 511-2. 2009.

[31] C.-W. Lee, A. Afzalian, N. D. Akhavan, I. Ferain, N D Akhavan, R. Yan, P. R. Razavi, R. Yu, R. T. Doria and J. P. Colinge, "Low subthreshold slope in junctionless multigate transistor", Appl. Phys. Lett., vol. 96, 102106, 2010.

[32] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors", Solid State Electron., vol. 54, no. 2, pp. 97–103, Feb. 2010.

[33] R. T. Doria, M. A. Pavanello, R.D. Trevisoli, M. de Souza, C. W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti and J. P. Colinge, "Junctionless multiple- gate transistors for analog applications", IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2511–2519, 2011.

[34] S. M. Wen and C. O. Chui, "CMOS junctionless field-effect transistors manufacturing cost evaluation", IEEE Trans. on Semiconductor Manuacturing, vol. 26, no. 1, pp. 162–168, Feb.

2013.

[35] S. Cho, K. R. Kim, B. G Park, I. M. Kang, "RF performance and small signal parameter extraction of junctionless silicon nanowire MOSFET", IEEE Trans. Electron Devices, vol. 58, no. 5, pp. 1388–1396, 2011.

[36] A. N. Nazarov, I. Ferain, N. D. Akhavan, P. Razavi, R. Yu and J.P. Colinge",Random telegraph-singal noise in junctionless transistors", Appl. Phys Lett., vol. 98, pp. 092111, 2011.

[37] W. Cheng, A. Teramoto and T. Ohmi, "Suppression of 1/f Noise in accumulation mode FD-SOI MOSFETs on Si (100) and (110) surfaces", AIP Conf. Proc., vol. 1129, no. 1, pp. 337-340, Apr. 2009.

[38] S. Takagi, A. Toriumi, M. Iwase and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part I-effects of substrate impurity concentration", IEEE Trans. Electron Devices, vol. 41, no. 12, pp. 2357–2362, Aug. 2011.

[39] S. Takagi, A. Toriumi, M. Iwase and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of substrate impurity concentration", IEEE Trans. Electron Devices, vol. 41, no. 12, pp. 2363–2368, Aug. 2011.

[40] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov and R. T. Doria, "Reduced electric field in junctionless transistors", Appl. Phys. Lett. vol. 96, pp. 073510–3, 2010.

[41] S.-J. Choi, D.-I. Moon, S. Kim, J. Duarte and Y.-K. Choi, "Sensitivity of threshold voltage to nanowire width variation in junctionless transistors", IEEE Electron Device Lett., vol. 32, no. 2, pp. 125–127, Feb. 2011.

[42] C.W. Lee, I. Ferain, A. Afzalian, R. Yan, N.D. Akhavan, P. Razavi and J. P. Colinge, "High temperature performance of silicon junctionless MOSFET", IEEE Trans. Electron Devices, vol. 57, no 3, pp. 620–625, Mar. 2010.

[43] R. Yan, D. Lynch, T. Cayron, D. Lederer, A. Afzalian, C. W. Lee, N. Dehdashti and J. P. Colinge, "Sensitivity of trigate MOSFETs to random dopant induced threshold voltage fluctuations", Solid-State Electron., vol. 52, pp. 1872–1876, 2008.

[44] A. Gnudi, S. Reggiani, E. Gnani and G. Baccarani, "Analysis of threshold voltage variability due to random dopant fluxtuations in juctionless FETs", Electron Device Lett., vol. 33, no. 3, pp. 336–338, Mar. 2012.

[45] C. J. Su, T.-I. Tsai, Y.-L. Liou ; Z.-M. Lin, H.-C. Lin and T.-S. Chao, "Gate-all-around junctionless transistors with heavily doped polysilicon nanowire channels", Electron Device Lett. vol. 32, no. 4, pp. 521–523, 2011.

[46] J. P. Duarte, S. J. Choi, D.I. Moon and Y.K. Choi, "Simple analytical bulk current model for long-channel double-gate junctionless transistors", IEEE Trans. Electron Devices, vol. 32, no. pp. 704–706, 2011.

[47] D. Ghosh, M. S. Parihar, G. A. Armstrong and A. Kranti, "High-performance junctionless

MOSFETs for ultralow-power analog/RF applications", IEEE Electron Device Lett., vol. 33, no. 10, pp. 1477–1779. Oct. 2012.

[48] Atlas User's Manual: Device Simulation Software, Version 3.8.18.R.2014

[49] Y. Hashim, O. Sidek, "Nanowire dimensions effect on ON/OFF current ratio and sub-threshold slope in silicon nanowire transistors", J. Nanosci. Nanotechnol. vol. 12, no. 9, pp. 7101-4, Sep. 2012.

[50] F. Silvera. D. Flandre, and P. G. A. Jespers, "A gm/Ids based methodology for the design of CMOS analog circuits an dits application to the synthesis of a silicon-on-insulator micropower OTA", IEEE J. Solid State Circuits, vol. 31, no. 9, pp. 1314–1319, Sep. 1996.

[51] J. T. Park, J. Y. Kim, C.W. Lee, J.P. Colinge, "Low temperature Conductance oscillations in junctionless nanowire transistors", Applied Physics Lett., vol. 97, pp. 172101–2, Oct. 2010.

[52] C.-W Lee, D. Lederer, A. Afzalian, R. Yan, N. Dehdashti, W. Xiong, et al., "Comparison of contact resistance between accumulation–mode and inversion-mode multigate FETs", Solid-State Electron, vol. 52, no. 11, pp. 1815-1821, 2008.

[53] S.M. Sze, Physics of semiconductor devices, 2nd ed., New York, Wiley, pp. 28, 1981.

[54] T. Skotnicki, F. Boeuf, "How can high mobility channel materials boost or degrade performance in advanced CMOS" Symposium on VLSI Technology Digest of Technical Papers, pp. 153–154, Honolulu, Hawaii, USA, Jun. 2010.

[55] J.-P. Colinge, A. Kranti, R. Yan, I. Ferain, N. D. Akhavan, P. Razavi, C.-W. Lee, R. Yu and C. Colinge, "A simulation comparison between junctionless and inversion-mode MuGFETs" ECS Trans., vol. 35, no. 5, pp. 63–72, 2011.

[56] A. Hokazono, S. Balasubramanium, K. Ishimaru, H. Ishiuchi, C. Hu, and T.-J. K. Liu, "MOSFET Hot-Carrier Reliability Improvement by Forward-Body Bias." IEEE Electron Device Lett., vol. 27, pp. 605–608, 2006.

[57] S. Saurabh, M. J. Kumar, "Estimation and compensation of process-induced variations in nanoscale tunnel field effect transistors for improved reliability," IEEE Trans. on Device and Materials Reliability, vol. 10, pp. 390–395, 2010.

[58] M. –C. Jeng, J. Chung, A.T. Wu, T. Y. Chan, J. Moon, G. May, P. K. Ko and C. Hu, "Performance and hot-electron reliability of deep-submicron MOSFETS," IEEE IEDM, San Francisco, pp. 1–4, 1987.

[59] S. Y. Chen, C. H. Tu, J. C. Lin, P. W. Kao, W. C. Lin, Z. W. Jhou, J. Ko and H. S. Haung, "Temperature effects on the hot carrier induced degradation of pMOSFETs." IEEE IIRW, California, pp. 1–4, 2006.

[60] R. Gautam, M. Saxena, R. S. Gupta and M.Gupta, "Hot-carrier reliability of gate-all-around MOSFET for RF/Microwave applications," IEEE Trans. on Device and Materials Reliability, vol. 13, pp. 245–251, 2013.

[61] W. Hansch, "Modeling hot carrier reliability of MOSFET: What is necessary and what is possible?" IEEE IEDM, San Francisco pp. 1–4, 1992.

[62] S.C. Williams, K. W. Kim, M.A. Littlejohn and W.C. Holton, "Analysis of hot-electron reliability and device performance in 80-nm double-gate SOI n-MOSFETs," IEEE Trans. Electron Devices, vol. 46, pp. 1760–1767, 1999.

[63] Y. Pratap, S. Haldar, R. S. Gupta and M. Gupta, "Performance evaluation and reliability issues of junctionless CSG MOSFET for RFIC design," IEEE Trans. on Device and Materials Reliability, vol. 14, pp. 418–425, 2014

[64] U. Abelein, M. Born, K. K. Bhuwalka, M. Schindler, M. Schlosser, T. Sulima and I. Eisele, "Improved reliability by reduction of hot-electron damage in the vertical impact-ionization MOSFET (I-MOS)," IEEE Electron Device Lett., vol. 28, pp. 65–67, 2007.

[65] R. Trevisoli, R. T. Doria, M. de Souza and M. A. Pavanello, "Substrate Bias Influence on the Operation of Junctionless Nanowire Transistors," IEEE Transactions on Electron Devices, vol. 61, no. 5, pp. 1575–1582, 2014

[66] S. M. Lee and J. T. Park, "The Impact of Substrate Bias on the Steep Subthreshold Slope in Junctionless MuGFETs," IEEE Transactions on Electron Devices, vol. 60, no. 11, pp. 3856-3861, 2013

[67] S. Gundapaneni, S. Ganguly, A. Kottantharayil, "Bulk planar junctionless transistor (BPJLT): An attractive device alternative for scaling", IEEE Trans. Electron Devices, vol. 32, pp. 261–263, 2011.

[68] R. Yan, D. Lynch, T. Cayron, D. Lederer, A. Afzalian, C. W. Lee, N. Dehdashti and J. P. Colinge, "Sensitivity of trigate MOSFETs to random dopant induced threshold voltage fluctuations", Solid-State Electron., vol. 52, pp. 1872–1876, 2008.

[69] J. T. Park, J. Y. Kim, C.W. Lee, J.P. Colinge, Low temperature conductance oscillations in junctionless nanowire transistors." Applied Physics Letters, vol. 97, pp. 172101–6, 2010.

[70] C. W. Lee, A. Borne, L. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi and J. P. Colinge, "High-temperature performance of silicon junctionless MOSFETs," Trans. Electron Devices, vol. 57, pp. 620–625, 2010.

[71] M. Willanderi, M. Frieseli, Q. U. Wahab, B. Straumal, "Review: Silicon carbide and diamond for high temperature device applications," Journal of Materials Science: Materials in Electronics, vol. 17, pp. 1– 25, 2006.

[72] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett and B. J. Blalock, "A High Temperature Silicon Carbide MOSFET Power Module With Integrated Silicon-On-Insulator-Based Gate Drive," IEEE Trans. on Power Electron., vol. 30, no. 3, pp. 1432–1445, Mar. 2015.

[73] M. Ostling, R. Ghandi and C.-M. Zetterling "SiC power devices – present status, applications and future perspective," Proceedings of the 23rd International Symposium on Power Semiconductor Devices &IC's, pp. 10–15, San Diego, CA, 2011.

[74] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iñiguez, and F. Prégaldiny, "Charge- based modeling of junctionless double- gate field- effect transistors", IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2628–2637, Aug. 2011.

[75] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the junctionless nanowire FET", IEEE Trans. Electron Devices, vol. 58, no. 9, pp. 2903–2910, Sep. 2011.

[76] J. P. Duarte, S.-J. Choi and Y.-K. Choi, "A full-range drain current model for double –gate junctionless transistors", IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4219-4225, Dec. 2011.

[77] Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu and Y. Zhou, "Surface – potential – based drain current model for long-channel junctionless double - gate MOSFETs", IEEE Trans. Electron Devices, vol. 59, no. 12, pp. 3292-3298, Dec. 2012.

[78] T. - K. Chiang, "A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs", IEEE Trans. Electron Devices, vol. 59, no. 9, pp. 2284-2289, Sep. 2012.

[79] F. Lime , E. Santana and B. Iñiguez, "A simple compact model for long-channel junctionless double gate MOSFETs", Solid State Electron., vol. 80, pp. 28-30, Feb. 2013.

[80] J. P. Duarte, M.-S. Kim, S.-J. Choi and Y.-K. Choi, "A compact model of quantum electron density at the subthreshold region for double-gate junctionless transistors", IEEE Trans. Electron Devices, vol. 59, no. 4, pp. 1008-1012, Apr. 2012.

[81] J. P. Duarte, S.-J. Choi, D.-I. Moon and Y.-K. Choi, "A nonpiecewise model for long-channel junctionless cylindrical nanowire FETs", IEEE Electron Device Lett., vol. 33, no. 2, pp. 155–157, Feb. 2012.

[82] R. D. Trevisoli, R. T. Doria, M. Souza and M. A. Pavanello, "A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors", Solid-State Electron., vol. 90, pp. 12-17, Dec. 2013.

[83] R. D. Trevisolia, R. T. Doria and M. A. Pavanelloc, "Analytical model for the threshold voltage in junctionless nanowire transistors of different geometries", ECE Transactions", vol. 39, no. 1, pp. 147-154, 2011.

[84] R. D. Trevisoli, R. T. Doria, M. de Souza and M. A. Pavanello, "Accounting for short channel effects in the drain current modeling of junctionless nanowire transistors", ECS Trans., vol. 49, no. 1, pp. 207-214, 2012.

[85] A. Cerdeiral, M. Estradal, R. D. Trevisoli, R. T. Doria, M. Souza and M. A.. Pavanello, "Analytical model for potential in double-gate juntionless transistors", Symposium on Microelectronics Technology and Devices (SBMicro), pp. 1–3, 2013.

[86] A. Yesayan, F. Prégaldiny and J.-M. Sallese, "Explicit drain current model of junctionless double-gate field-effect transistors", Solid-State Electron., vol. 89, pp. 134–138, Nov. 2013.

[87] G. Hu, P. Xiang, Z. Ding, R. Liu, L. Wang and T.-A. Tang, "Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors", IEEE Trans. Electron Devices, vol. 61, no. 3, pp. 688–695, Mar. 2014.

[88] J.-H. Woo, J.-M. Choi and Y.-K. Choi, "Analytical threshold voltage model of junctionless double-gate MOSFETs with localized charges", IEEE Trans. Electron Devices, vol. 60, no. 9, pp. 2951-2955, Sep. 2013.

[89] C. Li, Y. Zhuang, S. Di and R. Han, "Subthreshold behavior models for nanoscale short-channel junctionless cylindrical surrounding-gate MOSFETs", IEEE Trans. Electron Devices, vol. 60, no. 11, pp. 3655-3662, Sep. 2013.

[90] R. D. Trevisoli, R. T. Doria, M. Souza, S. Das, I. Ferain and M. A. Pavanello, "Surface-potential-based drain current analytical model for triple-gate junctionless nanowire transistors", IEEE Trans. Electron Devices, vol. 59, no. 12, pp. 3510-3518, Dec. 2012.

[91] A. Cerdeira, M. Estrada, B. Iniguez, R. D. Trevisoli, R. T. Doria, M. de Souza, and M. A. Pavanello, "Charge-based continuous model for long-channel symmetric double-gate junctionless transistors", Solid-State Electron., vol 85, pp. 59-63, Jul. 2013.

[92] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iñiguez and F. Prégaldiny, "Charge-based modeling of junctionless double-gate field-effect transistors", IEEE Trans. Electron Devices, vol. 58, no. 8, pp. 2628-2637, Dec.2011.

[93] Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu and Y. Zhou, "Surface – potential – based drain current model for long-channel junctionless double - gate MOSFETs", IEEE Trans. Electron Devices, vol. 59, no. 12, pp. 3292-3298, Dec. 2012.

[94] B. Ray, S. Mahapatra, "Modeling of channel potential and subthreshold slope of symmetric double - gate transistor", IEEE Trans. Electron Devices, vol. 56, no. 2, pp. 260-266, Feb. 2009.

[95] X. Jin, X. Liu, M. Wu, R. Chuai, J.-H. Lee and J.-H. Lee, "Modelling of the nanoscale channel length effect on the subthreshold characteristcs of junctionless field-effect transistors with a symmetric double-gate struture", J. Phys. D: Appl. Phys., vol. 45, pp. 375102-7, 2012.

[96] A. Gnudi, S. Reggiani, E. Gnani and G. Baccarani, "Semianalytical model of the subthreshold current in short-channel junctionless symmetric double-gate field-effect transistors", IEEE Trans. Electron Devices, vol. 60, no. 4, pp. 1342-1348, Apr. 2013.

[97] M.-L. Chen, W.-K. Lin and S.-F. Chen, "A new two-dimensional analytical model for nanoscale symmetrical tri–material gate stack double gate metal-oxide-semiconductor field effect transistors", Jpn. J. Appl. Phys., vol. 48, no. 10, pp. 1045031–7, Oct. 2009.

[98] C. Jiang, R. Liang, J. Wang and J. Xu, "A two-dimensional analytical model for short channel junctionless double-gate MOSFETs", AIP Advances, vol. 5, pp. 0571221-12, May. 2015.

[99] X. Jin, Xi Liu, H. Kwon, J. Lee and J. Lee, "A subthreshold current model for nanoscale short channel junctionless MOSFETs applicable to symmetric and asymmetric double-gate structure", Solid-State Electronics, vol. 82, pp. 77-81, Apr. 2013.

[100] T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region", Solid-State Electronics, vol. 90, pp. 107-115, Mar. 2013.

[101] H. A. E Hamid, J. R.Guitart and B. Iniguez, "Two-dimensional analytical threshold voltage and subthreshold swing models of undoped symmetric double-gate MOSFETs", IEEE Trans. Electron Devices, vol. 54, no. 6, pp. 1402–1408, Jun. 2007.

[102] X. Liang, Y .Taur, "2-D Analytical solution for SCEs in DG MOSFETs", IEEE Trans. Electron Devices, vol. 51, no. 8, pp. 1385–91, Aug. 2004.

[103] T. Holtij, M. Schwarz, A. Kloes and B. Iniguez, "2D analytical potential modeling of junctionless DG MOSFETs in subthreshold region including proposal for calculating the threshold voltage", 13th International Conference on Ultimate Integration on Silicon (ULIS), pp. 81 – 84, 2012.

Publications

Journals

[1] **Ratul Kr. Baruah**, Roy P. Paily, "A surface-potential based drain current model for short-channel symmetric double-gate junctionless transistor", Journal of Computational Electronics, Springer, vol. 15, no. 1, pp. 45–52, 2016.

[2] **Ratul Kr. Baruah**, Roy P. Paily, "Silicon Carbide based Double-gate Junctionless Transistor for High Temperature Applications", Journal of Electronic Materials, (Under review).

Conferences

[3] **Ratul Kr. Baruah**, Roy P. Paily, "Impact of Active Well Biasing on Process-Induced Variations of a Bulk Planer Junctionless Transistor", ICEE 2016, Dec. 27-30, IIT Bombay

[4] Rekib Uddin Ahmed and **Ratul Kr. Baruah**, "Modeling of Potential and Threshold Voltage in presence of Hot-Carriers for Short-Channel Double-Gate MOSFET", EDCAECT, Oct. 8-10, 2015, Gauhati University, India.

Some other publications in this field that are based on facilities of the said project

[6] **Ratul Kr. Baruah**, Roy P. Paily, "The Effect of High-k Gate Dielectrics on Device and Circuit Performances of a Junctionless Transistor", Journal of Computational Electronics, Springer, vol. 14, no. 2, pp. 492–499, 2015.

[7] **Ratul Kr. Baruah**, Roy P. Paily, "A Dual-Material Gate Junctionless Transistor using high-k spacer for Enhanced Analog Performance", IEEE Transactions on Electron Devices, vol 61, no. 1, pp. 123–128, 2014.

UTILISATION CERTIFICATE

FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year) 2014 (21/03/13-31/03/14)

(To be given separately for each financial year ending on 31st March)

U.C pertains to

✓ appropriate box

✓First Release	Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the Impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given
   : *Amount* N/A
   : Letter/Order No
   : Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount)
   : *Amount* Rs 11,11,000/-
   : Letter/Order No SB/FTP/ETA-268/2012
   : *Date* 03/09/2013
6.b Interest earned, if any : N/A
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 9,85,000/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 9,64,045/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 20,955/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.)
    : Amount N/A
    :Cheque/DD No.
    :Date
11. Amount to be carried forward to the next financial year (if any) : Rs 20,955/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs 9,85,000/- of Non-Recurring grants-in-aid sanctioned during the year 2013-14 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No SB/FTP/ETA-268/2012 dated 03/09/2013 and Rs N/A on account of unspent balance of the previous year, a sum of Rs 9,85,000/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 20,955/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —). Carry forward for next Financial year. 14.2.015

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
21/2/15

Signature of Registrar/Accounts officer
Date
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31ST MARCH)(year) **2015(01/04/14-31/03/2015)**
(To be given separately for each financial year ending on 31st March)

U.C pertains to ✓ *appropriate box*	✓First Release	Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given : *Amount* Rs 20,955/-
   : Letter/Order No
   : Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount) : *Amount* NIL
   : Letter/Order No
   : *Date*
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 20,955/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : NIL
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 20,955/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.) : Amount N/A
    : Cheque/DD No
    : Date
11. Amount to be carried forward to the next financial year (if any) : Rs 20,955/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs NIL of Non-Recurring grants-in-aid sanctioned during the year 2014-2015 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No — dated — and Rs 20,955/- on account of unspent balance of the previous year, a sum of Rs NIL has been utilised for the purpose for which it was sanctioned and that the balance of Rs 20,955/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —). Carry forward to next Financial year. ie 2016

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
21/2/17

Signature of Registrar/Account officer
Date
21/2/17
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year)2016(01/04/2015 - 31/03/2016)
(To be given separately for each financial year ending on 31st March)

U.C pertains to
✓ *appropriate box*

First Release	Second Release	Third Release	Fourth Release	Final Release
✓				

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given
   : *Amount* Rs 20,955/-
   : Letter/Order No
   : Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount)
   : *Amount* NIL
   : Letter/Order No
   : *Date*
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 20,955/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 9050/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 11,905/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.)
    : Amount N/A
    :Cheque/DD No.
    :Date
11. Amount to be carried forward to the next financial year (if any) : Rs 11,905/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs NIL of Non-Recurring grants-in-aid sanctioned during the year 2015-2016 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No — dated _____ and Rs 20,955/- on account of unspent balance of the previous year, a sum of Rs 9050/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 11,905/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —). Carry over to next Financial year. ie 01-04-16-2-9-17

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
28/2/17

Signature of Registrar/Account officer/
Date
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please **do not account** for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year) 2017(01/04/2016-02/09/2017)
(To be given separately for each financial year ending on 31st March)

U.C pertains to ✓ *appropriate box*	✓ First Release	✓ Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given : *Amount* Rs 11,905/- ; Letter/Order No ; Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount) : *Amount* NIL ; Letter/Order No ; *Date*
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 11,905/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : NIL
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 11,905/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.) : Amount N/A ; Cheque/DD No. ; Date
11. Amount to be carried forward to the next financial year (if any) : NIL

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs NIL of Non-Recurring grants-in-aid sanctioned during the year 2016-2017 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No — dated — and Rs 11,905/- on account of unspent balance of the previous year, a sum of Rs NIL has been utilised for the purpose for which it was sanctioned and that the balance of Rs 11,905/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no 048806 dated 10.03.17).

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
24/2/17

Signature of Registrar/Account officer
Date
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UC for Recurring Grants

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31ST MARCH)(year) **2014 (21/03/13-31/03/14)**
(To be given separately for each financial year ending on 31st March)

U.C pertains to
✓ *appropriate box*

First ✓Release	Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given : *Amount* NIL ; Letter/Order No ; Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount) : *Amount* Rs 1,26,000/- ; Letter/Order No SB/FTP/ETA-268/2012 ; *Date* 03/09/2013
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 1,26,000/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 63,208/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 62,792/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.) : Amount N/A ; Cheque/DD No. ; Date
11. Amount to be carried forward to the next financial year (if any) : Rs 62,792/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs 1,26,000/- of **Recurring** grants-in-aid sanctioned during the year 2013-2014 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No SB/FTP/ETA-268/2012dated 03/09/2013 and Rs NIL on account of unspent balance of the previous year, a sum of Rs 63,208/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 62,792/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —) OR will be adjusted towards the **Recurring** grants-in-aid payable during the next year i.e. 2015. Carry over to next Financial year.

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
22/2/17

Signature of Registrar/Account officer
Date
21/2/17
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UC for Recurring Grants

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year) 2015(01/04/14-31/03/2015)
(To be given separately for each financial year ending on 31st March)

U.C pertains to
✓ *appropriate box*

✓ First Release	Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given : *Amount* Rs 62,792/-
   : Letter/Order No
   : Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount) : *Amount* NIL
   : Letter/Order No
   : *Date*
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 62,792/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 14,106/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 48,686/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.) : Amount NIL
    :Cheque/DD No.
    :Date
11. Amount to be carried forward to the next financial year (if any) : Rs 48,686/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs NIL of Recurring grants-in-aid sanctioned during the year 2014-2015 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No — dated — and Rs 62,792/- on account of unspent balance of the previous year, a sum of Rs 14,106/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 48,686/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —) OR will be adjusted towards the Recurring grants-in-aid payable during the next year i.e. 2016. Carry over to next Financial year.

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date 22/2/17

Signature of Registrar/Account officer
Date 21/3/17
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please **do not account** for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year) 2016(01/04/2015-31/03/2016)
(To be given separately for each financial year ending on 31st March)

U.C pertains to
✓ *appropriate box*

✓First Release	Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA-268/2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given
   : *Amount* Rs 48,686/-
   : Letter/Order No
   : Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount)
   : *Amount* Rs. 2,00,000/-
   : Letter/Order No SERB/F/4286/2015-2016
   : *Date* 21/09/2015
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 2,48,686/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 1,70,032/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 78,654/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.)
    : Amount N/A
    :Cheque/DD No.
    :Date
11. Amount to be carried forward to the next financial year (if any) : Rs 78,654/-

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs 2,00,000/- of Recurring grants-in-aid sanctioned during the year 2015-2016 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No SERB/F/4286/15-16 dated 21/09/2015 and Rs 48,686/- on account of unspent balance of the previous year, a sum of Rs 1.70.032/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 78.654/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no — dated —) OR will be adjusted towards the **Recurring grants-in-aid payable during the next year** i.e. 2017 (1.4.16-2.9.16). Carry over to next Financial year.

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
22/2/17

Signature of Registrar/Account officer
Date
2/3/17
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____

UC for Recurring Grants

UTILISATION CERTIFICATE
FOR THE FINANCIAL YEAR - (ENDING 31st MARCH)(year) 2017(01/04/2016-02/09/2016)
(To be given separately for each financial year ending on 31st March)

U.C pertains to
✓ *appropriate box*

✓ First Release	✓ Second Release	Third Release	Fourth Release	Final Release

Is the UC provisional : YES / NO

1. Title of the Project/ Scheme : To study the impact and compensation of process-induced variations in junctionless transistors for improved reliability
2. Name of Principal Investigator : Dr. Ratul Kumar Baruah
3. Implementing Institution : Tezpur University
4. SERB sanction order No & date : SB/FTP/ETA/268-2012 dated 03/09/2013
5. Amount brought forward from the previous financial year quoting SERB letter number and date in which the authority to carry forward the said amount was given : *Amount* Rs 78,654/- ; Letter/Order No ; Date
6a. Amount received during the financial year (Please give SERB letter/order no and date for the amount) : *Amount* NIL ; Letter/Order No ; *Date*
6.b Interest earned, if any : NIL
7. Total amount that was available for expenditure *Rs.* (excluding commitments) during the financial year (Sr. No. 5+6a+6b) : Rs 78,654/-
8. Actual Expenditure (excluding commitments) incurred during the financial year (upto 31st March) : Rs 57,612/-
9. Balance amount available at the end of the financial year (8-9):OR / Negative balance (If expenditure incurred is more than the funds released) : Rs 21,042/-
10. Unspent balance, if any, refunded to SERB (give details of cheque/DD No etc.) : Amount N/A ; Cheque/DD No. ; Date
11. Amount to be carried forward to the next financial year (if any) : NIL

Finance Officer
Tezpur University

UTILISATION CERTIFICATE

Certified that out of Rs NIL of Recurring grants-in-aid sanctioned during the year 2016-2017 in favour of Dr. Ratul Kumar Baruah under SERB letter/ order No —— dated _____ and Rs 78,654/- on account of unspent balance of the previous year, a sum of Rs 57,612/- has been utilised for the purpose for which it was sanctioned and that the balance of Rs 21,042/- remaining unutilised at the end of the year has been refunded to SERB (vide Cheque/DD no 048806 dated 10.03.17) OR will be adjusted towards the Recurring grants-in-aid payable during the next year i.e. NIL.

Certified that we have satisfied ourselves that the conditions on which the grants-in-aid was sanctioned have been fulfilled/ are being fulfilled and that we have exercised the following checks to see that the money was actually utilised for the purpose for which it was sanctioned.

Kinds of checks exercised:
1.
2.

Signature of PI
Date
21/2/17

Signature of Registrar/Account officer
Date
21/2/17
Finance Officer
Tezpur University

Signature of Head of Institution
Date
Registrar
Tezpur University

Guidelines for preparation of U.C

1. U.C should be only for the grants released by the SERB. Please do not account for Security deposits/other matching grants/account opening charges and miscellaneous items.
2. SERB Sanction No. and Dt should be accurately shown in the U.C.
3. Even if the grant is unutilized in the financial year in which the grant was released by SERB a NIL U.C needs to be forwarded to SERB along with a request for carrying forward the grant to the next financial year. Such grants which are carried forward must be shown in the subsequent U.C as carried forward grant and not amount received in the subsequent year (ref Sl No.5 on pre-page).

Science and Engineering Research Board

UC accepted has been accepted by

Signature _____

Name of the SERB Officer _____

Designation _____