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To: serbinfo1@gmail.com

Science and Engineering Research Board

(Statutory Body Established Through an Act of Parliament : SERB Act 2008)
Department of Science and Technology, Government of India

Closure acknowledgement to PI

SCIENCE & ENGINEERING RESEARCH BOARD (SERB)

(Statutory Body Established Through an Act of Parliament : SERB Act 2008)

Science and Engineering Research Board

3rd & 4th Floor, Block II

Technology Bhavan, New Mehrauli Road

New Delhi - 110016

File Number: SRG/2019/000660

Dated: 29-Feb-2024

Subject: Project titled " **Nanocavity-in-Body Tunnel Field Effect Transistor Architectures for Low Power Sensing Applications** "

Dear Dr. RUPAM GOSWAMI

The SERB has received the required financial documents and the same have been accepted.

PCR was evaluated by the Expert Committee. Grading - Very Good.

This file is closed officially. This is for your kind information.

Yours sincerely,

(Dr. Ramesh Vijayan)

Email: ms_es_srg@serbonline.in

Dr. RUPAM GOSWAMI

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A Closure Report for a Project under Start-up Research Grant

Science and Engineering Research Board

Government of India

Title of the Project
Nanocavity-in-Body Tunnel Field Effect Transistor Architectures for Low Power Sensing Applications

File No.
SRG/2019/000660 dt. 26 November 2019 & 15 December 2020

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1. Objectives

Objective 1

Simulation framework design and optimization of TFETs with nanocavity-in-body style of architecture for biosensing and explosive sensing.

Objective 2

Incorporation of non-ideal effects like steric hindrance and partial hybridization of target molecules in simulation

Objective 3

Investigation and analytical modeling of sensitivity parameters in proposed TFET sensors

Objective 4

Launch of a Graphical User Interface (GUI) for accessing the analytical models for proposed sensors

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2. Research Accomplishments

The research accomplishments are summarized here.

[A] Objective-related accomplishments

1. **Design of a nanocavity-in-body TFET as sensor:** The chief research accomplishment of the project is the successful design of a nanocavity-in-body TFET for sensing applications, and identification of the design metrics responsible for effective sensing. In this regard, the primary goal of shifting the dielectric-modulation based sensing from the gate structure to the body in order to reduce fabrication challenges has been successful as evident from TCAD simulations. Moreover, the discovery of the back-track electric field of an opposing nature around the nanocavity-semiconductor junction has led to interesting conclusions.
2. **Revival of the p-n junction based TFETs:** The *p-i-n* geometry of TFETs is considered to be the most explored one. However, the presence of Zener tunneling in a reverse-biased *p-n* junction motivated for the design of a TFET without the intrinsic region. Therefore, a double gate *n-p-n* architecture has been proposed where utilizing an elevated structure, double gates can be made available on the same side of the device unlike a double gate *p-i-n* TFET. Gate engineered architectures and interface trap reliability of the proposed geometry have been analyzed.
3. **Linear Regression Based Model for Threshold Voltage in TFETs:** For the first time, a linear regression based model has been developed for TFETs by mapping the threshold voltage to the tunneling width in the source-channel tunnel junction. This paves the way for an alternative style of prediction-based modeling which can be customized for a single TFET architecture. The only input that the user needs to provide to the system is the minimum tunneling width.
4. **Figure-of-Merit (FOM) for any FET:** The analysis of the parameters of any field effect transistor (FET) as a sensor involves the determination of its low power performance without etching any cavity. Researchers have been using qualitative comparison among different electrical parameters based on priority; however, no numerical value based system was available to analyze the performance of a device based on some standards. Therefore, one of the important research accomplishments of this project is to offer a single numerical value based figure-of-merit (FOM) for any field effect transistor.

[B] Publications

1. **International Journals (SCI/ SCIE):** 5

[1] Manan Mehta, and Rupam Goswami, "Perspectives on Dielectric Modulated Biosensing in Silicon Tunnel FETs", *Silicon* (2021). doi: https://doi.org/10.1007/s12633-021-00945-4

[2] Deepjyoti Deb, Rupam Goswami, Ratul Kr Baruah, Rajesh Saha, and Kavindra Kandpal, "Role of Gate Electrode in Influencing Interface Trap Sensitivity in SOI Tunnel FETs," Journal of Micromechanics and Microengineering, vol. 32, no. 4, 044006, 2022. doi: https://doi.org/10.1088/1361-6439/ac56e8

[3] Deepjyoti Deb, Rupam Goswami, Ratul Kr Baruah, Rajesh Saha, and Kavindra Kandpal, "Parametric Investigation and Trap Sensitivity of n-p-n Double Gate TFETs," Computers and Electrical Engineering, vol. 100, May 2022. doi: https://doi.org/10.1016/j.compeleceng.2022.107930 .

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[4] Vikas Kumar, Manoj Kumar Parida, Rupam Goswami, and Deepjyoti Deb, Journal of Electronic Materials, vol. 50, pp. 6015-6019, Sep. 2021. doi: https://doi.org/10.1007/s11664-021-09189-9 .

[5] Sambhavi Shukla and Rupam Goswami, ECS Journal of Solid-State Science and Technology, vol.9, 085001. doi: https://doi.org/10.1149/2162-8777/abb797

2. International Conferences: 2

[1] Deepjyoti Deb, Rupam Goswami, Ratul Baruah, Kavindra Kandpal, Rajesh Saha, 4th IEEE International Conference on Devices and Integrated Circuits (DevIC) 2021, Kalyani, India, 19-20 May 2021. doi: https://doi.org/10.1109/DevIC50843.2021.9455827

[2] Sujay Routh, Deepjyoti Deb, Rupam Goswami, and Ratul Kr. Baruah, "Junctionless Tunnel FET for High-Temperature Applications from an Analog Design Perspective", IEEE 5NANO, Kerala, April 28-29, 2022. doi: https://doi.org/10.1109/5NANO53044.2022.9828986

3. Edited Book: 01 (Collaborative Work)

[1] 'Contemporary Trends in Semiconductor Devices: Theory, Experiment and Applications', Eds. Rupam Goswami, and Rajesh Saha, SpringerNature. Doi: https://doi.org/10.1007/978-981-16-9124-9

[C] Research Personnels Trained: 03 (Three)

1. Through recruitment under project: 01 (One) JRF (*continuing as a PhD scholar, enrolled in Autumn 2021*)

2. Additional Training on TCAD platform

(a) B.E. Scholars: 01 (One)

(b) PhD Scholars: 01 (One)

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3. Experimental/ Theoretical Investigation carried out

(Full details of experimental set up, methods adopted, data collected supported by necessary table, charts, diagrams & photographs)

The experimental/ theoretical investigation carried out in this project is detailed here according to the following sections.

3.1. Literature Survey

Prior to setting up the methodology and the orientation of the project, a literature survey was carried out with focus on dielectric-modulated biosensors based on Tunnel FETs (TFETs), and their methods. The sensitivities of the dielectric-modulated biosensors extracted from the literature are tabulated in Table 3.1. It is important to note that the measurement conditions must be cited when the sensitivity is mentioned, because the sensitivity is a function of multiple parameters (gate voltage, drain voltage, charge, dielectric constant of biomolecules, and others). A total of 20 devices were analyzed, and the sensitivities were extracted from the existing works.

Table 3.1. List of DM TFET biosensors with details and approximate sensitivity

Sl.	TFET biosensor	Measurement conditions	Sensitivity
1	DM-TFET [1]	V_{GS}=1 V, V_{DS}=1 V, k=10, charge=0	~1×10^7
2	FG-TFET [2]	V_{GS}=1 V, V_{DS}=0.4 V, k=4, charge=0	~2×10^5
3	SG-TFET [2]	V_{GS}=1 V, V_{DS}=0.4 V, k=4, charge=0	~1×10^6
4	DM-TFET [3]	(Uniform PH) V_{GS}=2 V, V_{DS}=1 V, k=10 charge=0	4.55×10^6
5	DM-TFET [3]	(Non-uniform step profile) V_{GS}=2 V, V_{DS}=1 V, k=10, charge=0	6.00×10^5
6	Gate-on-Drain TFET [4]	V_{GS}=−1 V, V_{DS}=1 V, k=10, charge=-5×10^{11} cm^{-2}	1×10^{10}
7	Circular Gate (CG) TFET [5]	V_{GS}=1.2 V, V_{DS}=1 V, k=12, charge=-10^{11} cm^{-2}	5.23×10^7
8	Heterojunction (HJ) TFET [5]	V_{GS}=1.2 V, V_{DS}=1 V, k=12, charge=-10^{11} cm^{-2}	2.387×10^6
9	Circular Gate (CG) TFET [5]	V_{GS}=1.2 V, V_{DS}=1 V, k=12, charge=10^{12} cm^{-2}	1.31×10^8
10	Heterojunction (HJ) TFET [5]	V_{GS}=1.2 V, V_{DS}=1 V, k=12, charge=10^{12} cm^{-2}	3.382×10^6
11	SiGe-source TFET [6]	Ge composition 10%, V_{DS}=0.5 V; k=2.1,charge=0	~495
12	Charge Plasma JLTFET [7]	V_{GS}=1.5 V, V_{DS}=0.5 V; k=10, charge=0	~3×10^7
13	Charge Plasma JLTFET [7]	V_{GS}=1.5 V, V_{DS}=0.5 V; k=5, charge=-5×10^{11} cm^{-2}	~1×10^6
14	EDTFET [8]	V_{GS}=0.9 V, V_{DS}=0.5 V, k=12, charge=0	~ 1×10^9
15	EDTFET [8]	V_{GS}=0.9 V, V_{DS}=0.5 V, k=4, charge=-1×10^{11} cm^{-2}	~1×10^6
16	FG-TFET [2]	V_{GS}=1 V, V_{DS}=0.4 V, k= 4, charge=0	~0.70 (surface potential sensitivity)

17	SG-TFET [2]	V_{GS}=1 V, V_{DS}=0.4 V; k= 4, charge=0	~0.95 (surface potential sensitivity)
18	HJ GAA TFET [9]	V_{GS}=1.5 V, V_{DS}=0.5 V, k=3.57, charge=0	+0.77 (threshold voltage sensitivity)
19	HJ GAA TFET [9]	V_{GS}=1.5 V, V_{DS}=0.5 V, k=3.57, charge=+5×10^{15} m^{-2}	+0.202 V (threshold voltage sensitivity)
20	HJ GAA TFET [9]	V_{GS}=1.5 V, V_{DS}=0.5 V, k=3.57, charge=−5×10^{15} m^{-2}	+0.157 V (threshold voltage sensitivity)

3.2. Methodologies for Objective 1

3.2.1 Nanocavity-in-Body TFET for biosensors: *simulation strategy and architecture*

Simulation Strategy

Sentaurus Technology Computer Aided Design (TCAD) was used as the device simulation platform for designing the nanocavity-in-body Silicon TFET biosensors. The device was designed for dielectric-modulated sensing, where the biomolecules are immobilized in the nanocavity, and the dielectric constant of the region changes, leading to change in electrical parameters. Nanocavity is etched out in the body region in the channel as opposed to gate structure in conventional TFET biosensors.

The physics-based models employed in the TCAD simulations were band-to-band tunneling model, bandgap narrowing model, doping dependent mobility model, and Fermi-Dirac statistics. The sensitivity was evaluated for negatively charged biomolecules, and positively charged biomolecules. The architecture is shown in Figure 3.1 (*refer to the attached complete technical report.*)

The region of biomolecules were considered in the TCAD simulations by taking a custom material and designating property of dielectric constant to it. Additionally, the hybridization of the biomolecules in the cavity was represented by defining interface charges at the biomolecule/ SiO_2 interface.

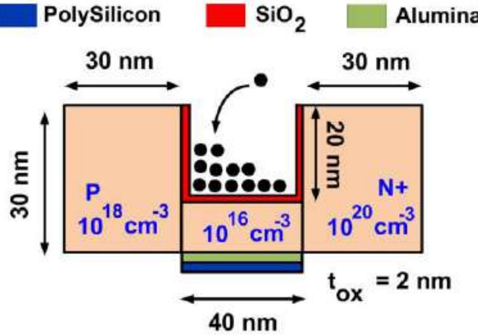

Figure 3.1. Architecture of nanocavity-in-body TFET considered in the TCAD simulation

Sensitivity Parameters and Fill Factor

The definition of sensitivity is crucial in a sensor. It is obvious that the change in dielectric constant of the cavity in the FET shall affect a number of electrical parameters of the sensor like threshold voltage, drain current and subthreshold swing. It is observed in FET-based sensors that the threshold voltage is the most affected electrical parameter which shows a distinct difference. So, we define a threshold voltage sensitivity as

$$S_{VT} = V_{TH,bio} - V_{TH,air} \quad (3.1)$$

where, $V_{TH,bio}$ is the threshold voltage of the sensor when its cavity is occupied with biomolecules and $V_{TH,air}$ is the common reference threshold voltage when the cavity of the sensor is empty, that is, filled with vacuum (k = 1).

Apart from the threshold voltage sensitivity, we also consider the drain current sensitivity which is expressed as

$$S_{ID} = {I_{D,bio}}/{I_{D,air}} \quad (3.2)$$

where $I_{D,bio}$ is the drain current of the FET when the cavity is filled with biomolecules and $I_{D,air}$ is the drain current when it is empty or filled with air.

There is another metric which is quite useful in considering practical cases in simulation environment of biosensors. Known as Fill Factor, it is defined mathematically as

$$FF = \frac{Volume\ occupied\ by\ biomolecules}{Total\ volume\ of\ the\ cavity} \times 100\% \quad (3.3)$$

Theoretically, to investigate the preliminary performance of the biosensor, the *FF* of a biosensor is assumed to be 100%. However, in practical scenarios, due to several reasons such as steric hindrance and partial hybridization, this is not the case.

Why nanocavity in-body geometry?

There are multiple reports on dielectric-modulated TFET biosensors, where the nanocavity for hybridization of biomolecules is located in the gate structure. A cavity is etched out of the gate dielectric, and the biomolecules are immobilized in the cavity. Theoretically, the

However, in a device like TFET, the semiconductor surface near the source-channel tunnel junction is highly sensitive as it is the site for the band-to-band tunnelling of carriers which contribute to the drain current. Etching out a cavity in the gate oxide, therefore, poses possibility of heavy process-induced damage to the surface, thereby, creating challenges in sensing capacities.

3.2.2. Interface trap reliability in TFETs

Motivation of the work

Generally, while analyzing the TFETs for sensing, its oxide/ semiconductor surface interface quality is not taken into account in simulations. Since the nanocavity-in-body architecture is a proposed alternative to the gate nanocavity based TFETs, therefore, understanding the impact of the interface traps on the performance of the device will lead to insight into the operation of these tunneling transistors, which will be beneficial for detailed design of both the categories of sensing architectures. The gate electrode in a TFET is the most important electrode as it is responsible for creating the tunneling window in the source-channel tunnel junction, and its impact on the trap sensitivity of the TFETs was analyzed.

Methodology and Simulation Strategy

All simulations were performed using Synopsys Inc.'s Sentaurus TCAD industrial simulator. Fermi-Dirac statistics were utilized instead of Boltzmann statistics due to the existence of large doping concentrations. When extrinsic doping concentrations in Silicon semiconductors are above a certain threshold, band gaps are lowered. As a result, the band gap narrowing model was selected. Due to the high levels of doping, a doping-dependent mobility model was used. To account for quantum tunneling phenomena, a calibrated Schenk band-to-band tunneling (BTBT)

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model was utilized. The TFET was calibrated with the experimental data from the TFET in Choi et al [10] as shown in Figure 3.2, and the model parameters obtained after calibration are as follows as A = 7 × 10^{21}cm^{-1} s^{-1} V^{-2}, B = 1.25 × 10^{7} eV$^{-1.5}$V/cm, and hω = 18.6meV.

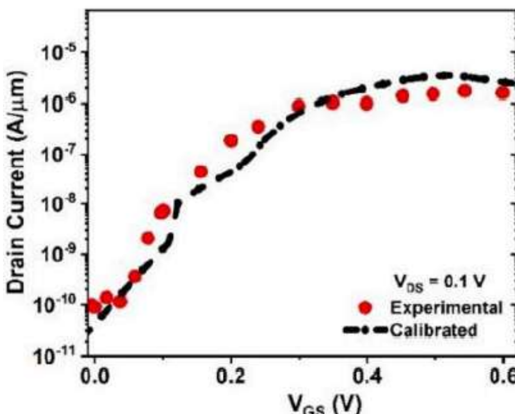

Figure 3.2. Calibration of the simulation setup using [2] experimental findings.

The technique used in the study summarizes the relevance of gate terminals in the case of interface trap effects for the SOI tunnel field effect transistor. The sensitivity of the design to semiconductor/oxide interface traps was investigated using a Gaussian trap distribution. Two types of traps were considered: donor-like traps and acceptor-like traps, and a trap sensitivity parameter of $\frac{\left(I_{D_{no\ traps}} - I_{D_{traps}}\right)}{I_{D_{no\ traps}}} X\ 100\ \%$ was specified, and the value was plotted against gate-to-source voltage for various parameters. The Gaussian trap distribution has the highest sensitivity of the three and is regarded as one of the most realistic depictions of traps in practice.

Methodical Investigation

Figure 3.3 shows a diagram of the methods used in this paper. The full set of methods was separated into three stages of analysis, as illustrated. Part 1 covered broad preliminary assessments of the impacts of trap concentration, peak position, and drain voltage on transfer characteristics. The primary goals of the work were addressed by the studies indicated in Part 2 including variations in geometrical parameters and work-function connected to the gate construction. Part 3 involved the device's noise response in the presence of three noise sources.

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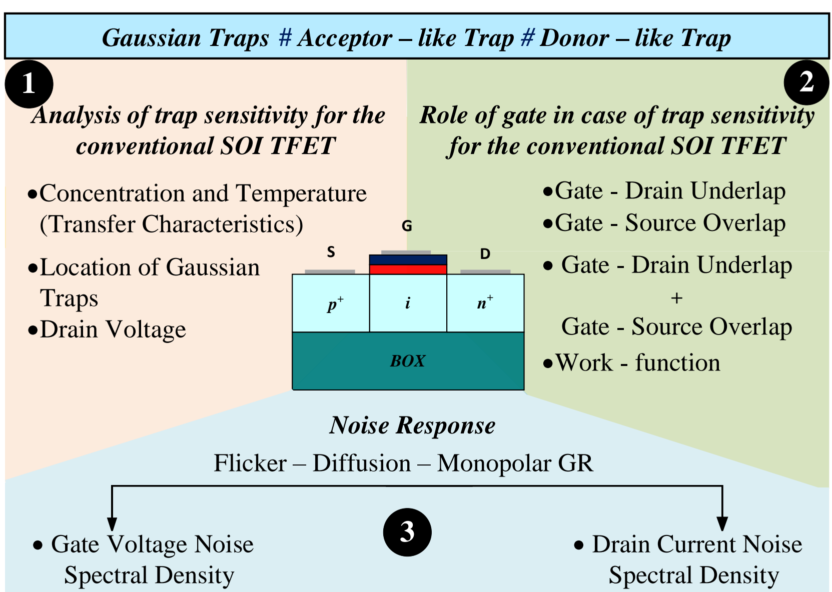


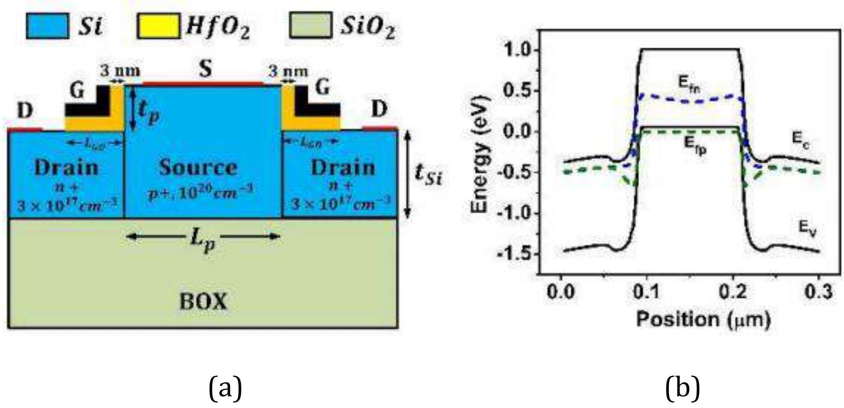
Figure 3.3. Methodology of the investigation for Sec. 2.2

3.2.3. Alternative TFET geometries

Architectures

(a) Double Gate n-p-n TFET

A TFET structure is designed based on single p-n junctions. The structure is an n-p-n geometry just like a BJT but with reverse biased p-n junctions, and gate structures over both the junctions. The architecture of the proposed TFET is shown in Figure 3.4 (a). The architecture has two p-n junctions, and by reverse-biasing both junctions, tunneling can be achieved at a positive gate bias as evident from the energy band profile in on-state from Figure 3.4 (b). The architecture does not employ the conventional intrinsic region as channel, and hence, the doping concentrations of the drain regions must be optimized to counter the ambipolar current as well as maintain an appreciable I_{ON}. The gate dielectric thickness is kept constant at 3 nm for all simulations.



(a) (b)

Figure 3.4. (a) Schematic diagram of n-p-n TFET. (b) Energy band diagram of n-p-n SOI TFET in on state.

(b) *Junctionless TFET*

A junctionless TFET is shown in Figure 3.5 which can act as a prospective nanocavity-in-body TFET sensor. The temperature dependence of the junctionless TFET was analyzed and compared with that of the conventional *p-i-n* SOI TFET.

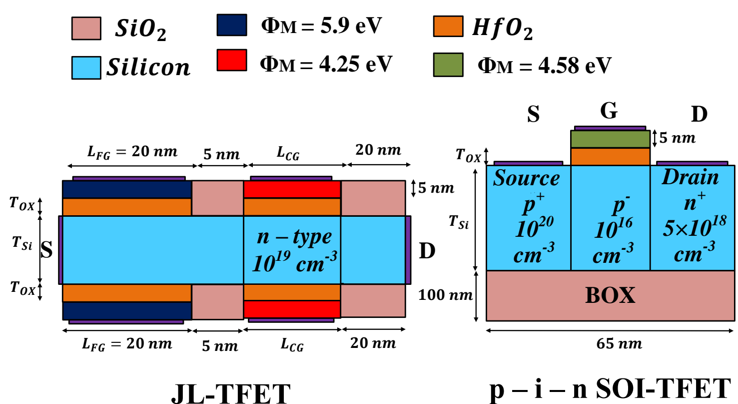


Figure 3.5. Schematic diagram for both JLTFET and p-i-n SOI TFET.

Methodology and Simulation Strategy

(a) *Double Gate n-p-n TFET*

Because the n-p-n design differs fundamentally from the traditional $p - i - n$ shape of TFETs, a systematic methodology is required to study device performance. The industrial simulator, Sentaurus TCAD from Synopsys Inc., was used for all simulations. Due to the presence of high doping concentrations, Fermi-Dirac statistics were used instead of Boltzmann statistics. Band gaps in Silicon semiconductors are reduced when extrinsic doping concentrations are above a particular threshold. As a consequence, the band gap narrowing model was chosen. Because of the high amounts of doping, a doping-dependent mobility model was adopted. A calibrated Schenk band-to-band tunneling (BTBT) model (*similar to Sec. 3.2.2*) was used to incorporate the quantum tunneling effects.

(b) *Junctionless TFET*

Carriers are tunneled using the nonlocal band-to-band tunneling (BTBT) concept. The bandgap narrowing (BGN) model is enabled because the substrate has been doped at high concentrations. The Shockley-Read-Hall (SRH) recombination model is employed because of the device's high impurity concentration, allowing for temperature dependence. Calibration of the simulated dataset is carried out by changing A_{path}, B_{path} and D_{path} band-to-band tunneling model, and the resultant parameters achieved after calibration are $A_{path} = 2.6 \times 10^6\ cm^{-3}\ s^{-1}$, $B_{path} = 4.2 \times 10^6\ Vcm^{-1}$, $D_{path} = -0.45\ eV$.[11]

Methodical Investigation

(a) *Double Gate n-p-n TFET*

To analyze the performance of the proposed device, parametric optimization in a double gate n-p-n SOI TFET was carried out in a serial fashion, using the first parameter as drain doping (N_{Drain}). Taking the optimized drain doping, further gate-on-drain length (L_{GD}) was optimized. Now considering the gate-drain underlap optimization, the work function (φ_M) was further optimized together with silicon thickness (t_{Si}), optimization of elevated

length of the source (t_p), and lastly, the optimization of source length (L_p). Detailed flowchart is shown below in Figure 3.6.

The optimized TFET from the first stage was subjected to three gate engineering approaches in the second phase. The dual gate dielectric, stack gate dielectric, and dual work function techniques were used, and the electrical properties of the three TFETs are explored and compared.

The sensitivity of the four designs to semiconductor-interface traps is assessed in the third stage by taking the Gaussian trap distribution into account. The peak concentrations and peak level placements of two types of traps, namely donor-like traps and acceptor-like traps, are altered. A trap sensitivity parameter was defined as $\frac{(I_{D_{no\ traps}} - I_{D_{traps}})}{I_{D_{no\ traps}}} X\ 100\ \%$ and was specified in relation to devices that did not have traps. The effect of trap-assisted tunnelling on device properties was also investigated.

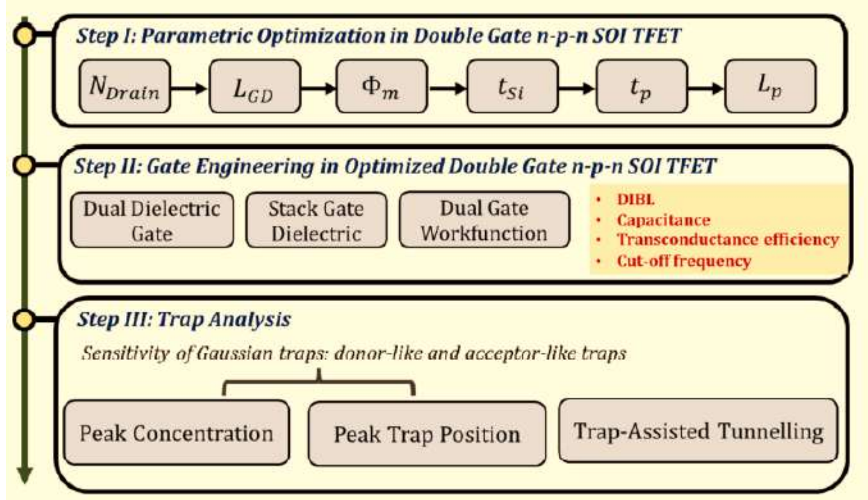


Figure 3.6. Flowchart illustrating the methodical investigation for Sec. 3.2.3.

(b) Junctionless TFET

By adjusting temperatures, the two TFET architectures' (Figure 3.5) performance has been examined from an analog design standpoint. Because more mobile carriers tunnel as the gate bias rises above the threshold voltage, the drain current rises exponentially.

3.3. Methodologies for Objective 2

The partial hybridization of biomolecules in the nanocavity is a practical scenario. The sensitivity of a sensor is theoretically reported at a fill factor of 100% which is a rare occurrence. Therefore, analyzing a device performance at reduced fill factors is important.

This objective, therefore, addresses this, and the analysis of fill factor was carried out in the TFET and thin film transistor (TFT) as sensors.

The methodology for the nanocavity-in-body TFET has already been described in Sec. 3.2.2. Here the methodology and simulation set-up for the TFT is mentioned here.

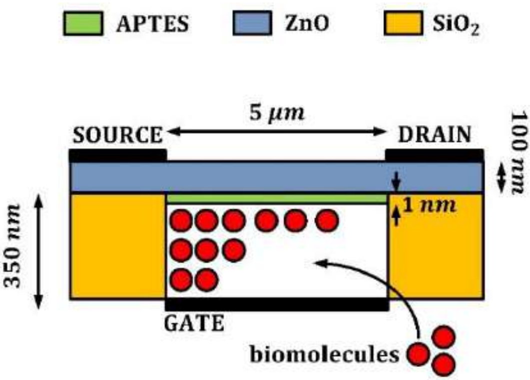


Figure 3.7. 2-D schematic of the bottom gate dielectric modulated ZnO TFT

A 2-D schematic of the device architecture is shown in Figure 3.7. A cavity is etched out of the gate dielectric to immobilize the biomolecules. In order to hybridize the biomolecules, a layer of APTES is used, its thickness being approximately 1 nm [21].

Methodology and Simulation Strategy

The methodology and simulation strategy for the TFET sensors are already described in Sec. 3.2.2. For the ZnO TFT based sensor, the simulations were performed on Sentaurus TCAD tool by Synopsys Inc. For the simulation, the Fermi-Dirac statistics, SRH recombination and bandgap narrowing effects were enabled.
The complete simulation strategy can be divided into two important steps.

- Firstly, the ZnO material is represented on TCAD by creating a material with the properties listed in Table 3.2.
- Since the ZnO is intrinsically n-type, so a doping concentration is used.
- Figure 3.8 (a) shows FESEM image of a 200 nm thick ZnO film deposited using RF magnetron sputtering at room temperature. Deposited ZnO film shows polycrystalline deposition with an average grain size of 25 nm. In polycrystalline material, grain boundaries act like trapping centres to the charge carriers. It is very complex to take the grain boundaries effect by taking its structure or morphology in account. However, a better way to include effect of grain boundaries trap densities is by approximating grain boundaries as deep and tail density of states in energy band-gap of a semiconductor. Hossain *et al.* approximated these trap density as a Gaussian distribution in the band-gap as a part of their analytical model of ZnO TFT [12]. The same formulation was adopted in the simulation of the TFT in this article, which is represented graphically in Figure 3.8 (b).

Table 3.2. Parameters used to represent ZnO on TCAD tool

Parameter	**Value**
ZnO Dielectric Constant	8.12
ZnO Bandgap	3.37 eV
ZnO Electron Affinity	4.29 eV
N-type doping in ZnO Layer	$1x10^{16}\ cm^{-3}$

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- The biomolecules were represented on the tool by considering a dielectric material in the cavity, whose dielectric constant is set to that of the target molecules.
- On getting immobilized in the cavity, there is a charge developed at the interface of the biomolecules/APTES. This was represented on the tool by defining a value of charge at the biomolecule equivalent dielectric/APTES interface.
- Two biomolecules, namely, streptavidin (k = 2.1) and protein (k = 4) were considered for the simulations [13-14]. The closeness of the dielectric constants of the two biomolecules was expected to assist in arriving at important conclusions regarding the performance of the proposed sensor.
- The term 'protein' was used in generic sense in the work. Since majority of the theoretical and experimental evidences have placed the dielectric constant protein between 1 and 6, so, a value of 4 was considered in the reported range [14].
- The values of charge were taken in accordance with the charge of a single strand DNA [13].

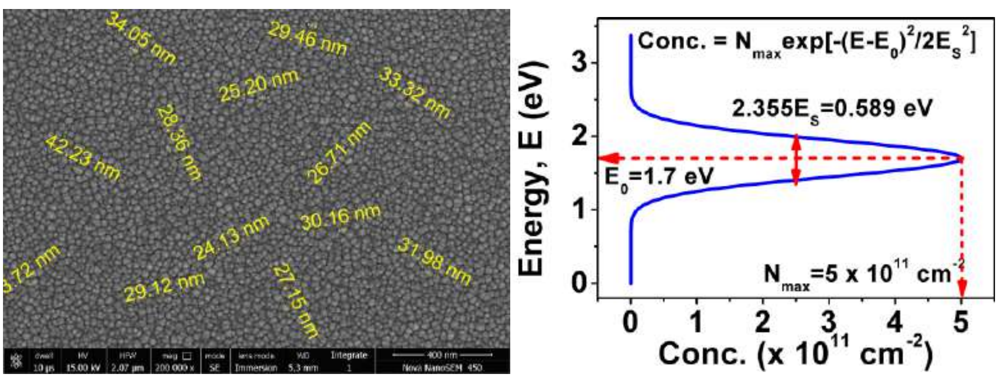

Figure 3.8. (a) FESEM image of a ZnO thin film deposited using RF sputtering showing the grains; (b) An effective Gaussian trap distribution at the SiO_2/ZnO interface of the proposed TFT to consider the effect of grain boundaries.

3.4. Methodologies for Objective 3

3.4.1. Threshold Voltage Extraction Model

The threshold voltage of a TFET is an important electrical parameter in sensing applications. A change in the gate dielectric constant or interface charge leads to a shift in the threshold voltage in TFETs, which is used as a measure of sensitivity of the sensor.

Methodical Investigation

- The chief focus was on prediction of threshold voltage parameter for low-power transistors as it benchmarks several parameters such as the on current (I_{ON}), off current (I_{OFF}).
    - The most commonly used approach by the experts is the transconductance method based on the gate-voltage intercept of the tangent drawn to the point of maximum transconductance in the transfer characteristic.
    - Another physics-based approach is the condition where the band bending becomes equal to the energy bandgap. However, physics-based approaches suffer from several drawbacks; such as high source doping introducing a bandgap narrowing factor in the source, resulting in different effective bandgaps in the source and channel regions. This creates an ambiguity in the bandgap condition to be applied because the energy band bending varies from the source to the channel region.
- To overcome such problems, we have introduced a more convenient method with lower computational complexity such as regression which was proposed based on a simple yet

novel algorithm that takes the tunneling width as its input parameter to estimate the minimum tunneling width at the threshold voltage.

- In an n −type TFET, with increasing gate-to-source voltage, the tunneling width reduces, and carrier tunneling from the valence band of the source to the conduction band of the channel primarily contributes to the tunneling current.
- The increase in gate voltage (V_{GS}) decreases the tunneling width (T_{min}). Now the change in tunneling width (T_{min}) changes the threshold voltage (V_{TH}) value which suggests that there is an inherent relationship between the threshold voltage (V_{TH}) of a TFET and the tunneling width (T_{min}).
- The relationship between the threshold voltage (V_{TH}) of a TFET and its tunneling width at the threshold voltage (W_{tmin}), is established, the threshold voltage of the TFET can be conveniently found by merely solving the surface potential. The proposed algorithm establishing this relationship is shown in Figure. 2 below

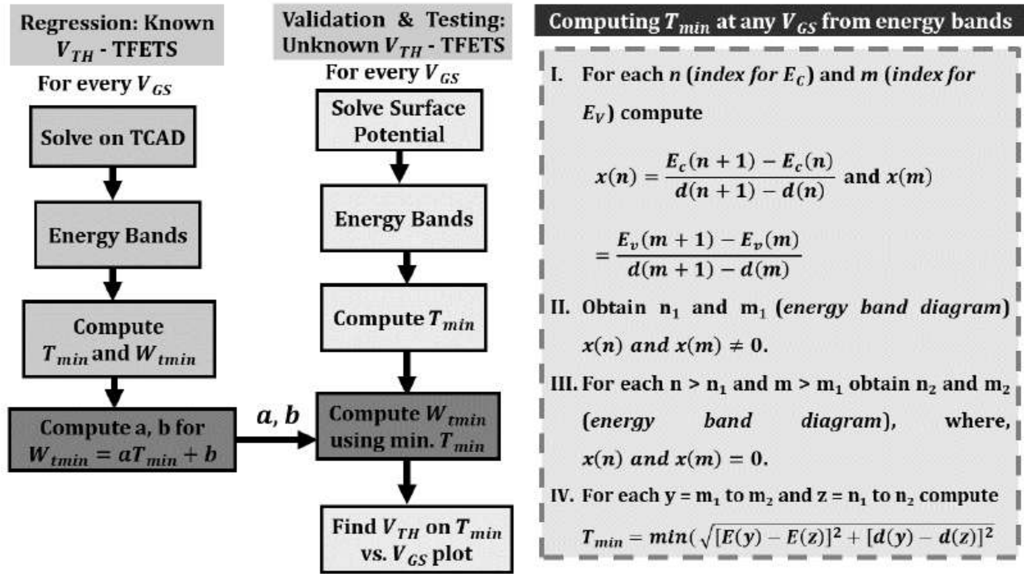

Figure 3.9. Flowchart of Linear regression-based method for extracting the threshold voltage of TFETs.

- To carry out this process, TFET architectures are divided into two categories: category A, TFETs for which threshold voltage (V_{TH}) values are known, and category B, TFETs for which threshold voltage (V_{TH}) values are unknown. A total of 27 TFET architectures were simulated using the Sentaurus TCAD industrial simulator from Synopsys Inc.
- For V_{GS} values ranging from 0 to 1 V and taking step size of 0.1, minimum tunneling width, (T_{min}), was calculated using the Euclidean distance method as illustrated in Figure 3.9.
- In the next step the threshold voltage is then extracted from the transfer characteristics, and (W_{tmin}), is computed from the energy bands. A linear relationship is then constructed as $W_{tmin} = aT_{min} + b$, and the unknown values of the coefficients a and b were computed using the known values of W_{tmin} and T_{min} previously reported for the set of 27 simulated devices. The optimized values of the coefficients a and b are were thus found to be 1.084 and 0.6211, respectively.
- To confirm this relationship with these coefficients, the linear expression was verified for 8 new TFET architectures belonging to category B. For this validation, the surface potential was solved using the Poisson equation and the values of T_{min} for each V_{GS} in the range from 0 V to

1 V are recorded. Now, since the linear relationship was valid for T_{min}, the minimum value of T_{min} could be used to obtain the value of W_{tmin}, which is the tunneling width at the threshold voltage.

3.4.2. A Figure-of-Merit for Low Power Devices

A figure-of-merit (FOM) is a quantitative measure of how suitable an architecture is for low-power applications. This applies to any FET and its applications including sensors. The objective of developing the FOM is to provide a mathematical metric to decide on the performance aspects of MOS devices for low-power applications. The mathematical expression of the FOM is proposed to be a function where I_{ON}, V_{TH}, SS and I_{ON}/ I_{OFF} ratio, and expressed below these parameters can be categorized into two sets depending on the nature of their definitions.

$$f = \left(\frac{I_{ON}}{I_{ON,IRDS}} + \frac{V_{GS,MAX} - V_{TH}}{\delta V_{GS,MAX}}\right)\frac{60}{SS} + \alpha . ln\left(\frac{I_{ON}}{I_{OFF}}\right) + ln\left(\left|n_{I_{AMBI}}\right|\right) \quad (3.4)$$

Where, $\alpha = \frac{\left(\frac{6}{\left|n_{I_{ON}}\right|}\right)}{\frac{6}{\left|n_{I_{ON}}\right|}}$ and the rest of the symbols are listed here.

Symbol	Meaning
I_{ON}	On current of the FET
$I_{ON,IRDS}$	IRDS reference on current (10^{-6} A/ µm)
$V_{GS,MAX}$	Maximum gate voltage
V_{TH}	Threshold voltage
SS	Subthreshold swing
I_{OFF}	Off-state current
$n_{I_{AMBI}}$	Order of ambipolar current
δ	Weighted parameter

The first set of parameters are concrete output parameters which can dominantly characterize the device. These include the on current (I_{ON}), off current (I_{OFF}), threshold voltage (V_{TH}) and subthreshold swing (SS). However, with the emergence of devices like Tunnel Field effect Transistors (TFETs), the ambipolar current has emerged as a matter of concern and can be included in the first set of parameters.
The second set of parameters consists of the derived parameters, which are inherent to the analytical studies of the device. These include parameters like surface potential, electric fields, band-to band tunneling and electron densities. To understand the physics of a new device, these parameters are used in explaining the nature or trend of the first set of parameters.

3.5. Methodologies for Objective 4

A graphical user interface application is designed for Android mobile phones containing information on the outcomes of the project. At the time of submission of this report, the initial work on the interface is ready, and the information is being loaded into the application. A screenshot of the design tool where the application is designed is shown in Figure 3.10. The primary objectives of launching a GUI are

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- To acquaint researchers working in the domain of dielectric-modulated TFETs with the concept of nanocavity-in-body TFET architecture.
- To provide an informative insight into the conclusions of the research undertaken in this project.

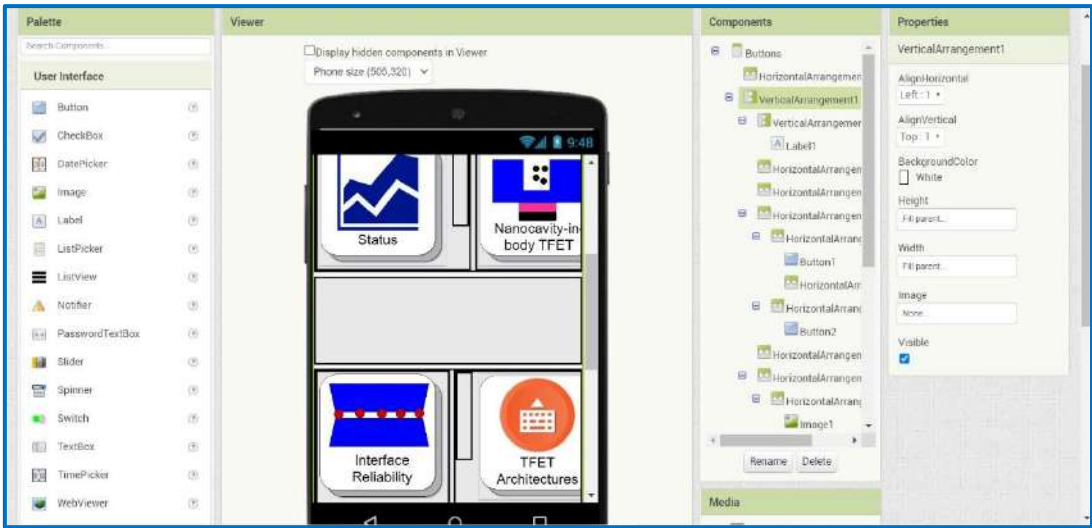


Figure 3.10. A screenshot of the application designer tool

4. Detailed Analysis of Result

(indicating contributions made towards increasing the state of knowledge in the subject)

The detailed analysis of results are described here according to the objectives in a similar manner as methodology.

4.1. Important Perspectives from Literature Survey

The key perspectives derived from the literature survey with reference to the existing literature on dielectric-modulated (DM) TFETs as biosensors, which motivate the objectives of the work are listed here.

- Process-induced defects (PIDs) pose a serious threat to the operation of a FET. The formation of a nanocavity in the gate dielectric which is carried out by etching on a previously deposited gate dielectric material, damages the gate oxide. Moreover, the risk of damaging the Silicon substrate at the surface as well as damages due to etching close to the tunnel junction may render the device unsuitable for application as a biosensor. So, etching a cavity in a TFET as a DM biosensor (Figure 4.1) must not degrade the sensitivity significantly which is the most challenging part.
- The presence of probes in the gate nanocavity close to the tunnel junction is very essential to influence a high sensitivity in the sensing device. Due to this, partial hybridization (PH) of biomolecules in the cavity was another concern for TFETs where the phenomenon of steric hindrance in nanocavity-based sensors restricts the entry of other molecules in the presence of initially hybridized molecules in the cavity (Figure 4.1). Theoretically, such conditions have been reported by assuming specific profiles of biomolecules in the cavity.

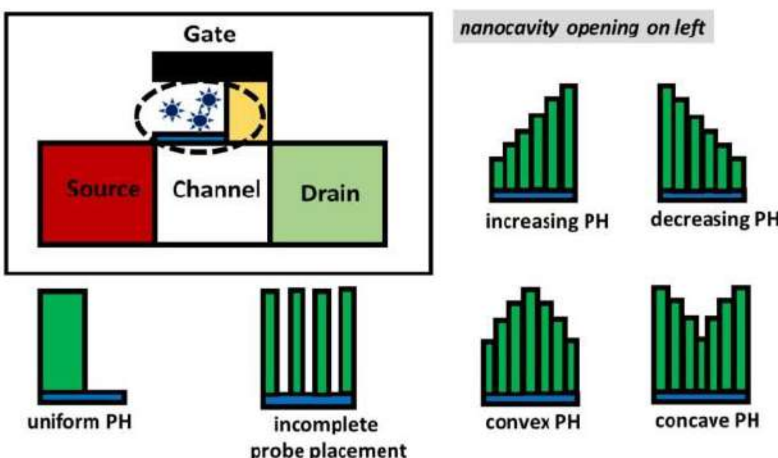


Figure 4.1. Cases of uniform PH, nonuniform PH (step profiles: increasing, decreasing, convex and concave), and probe placement scenarios in DM TFETs as biosensors used during TCAD simulation in reported works

- The phenomenon of partial hybridization (PH) reduces the sensitivity of the DM TFET biosensors due to the reduced fill factor of the cavity, the strategies for the fabrication of nanocavity of the biosensor should be taken up either in etching out a perfect cavity in the gate dielectric, which is tedious, and has the possibility of increased costs, or developing

efficient bias circuitry which can take into account the variations intelligently to produce results with acceptable tolerance levels.

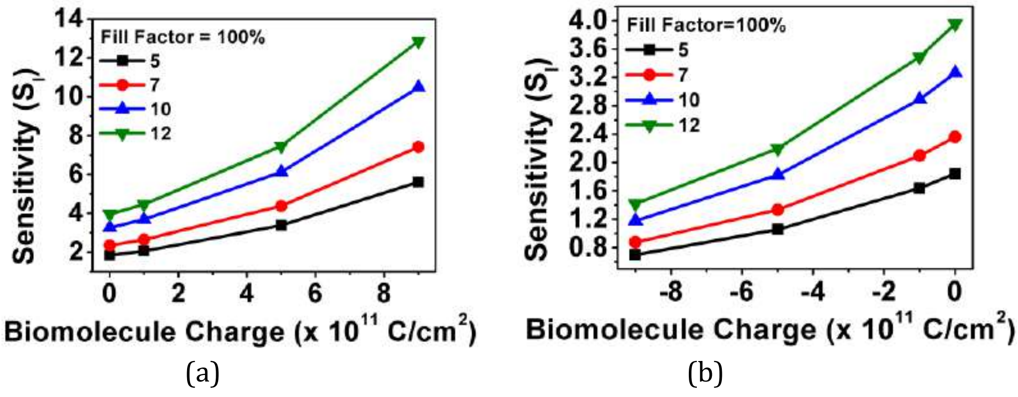
- An important measure which would be more beneficial is that the location of the nanocavity can be shifted from the gate region to other locations of the architecture, where the effect of dielectric modulation can be exploited. This shall hugely alleviate the problems of process-induced damages in the gate dielectric region, and maintain the fabrication cost at acceptable levels.
- The location of the cavity must be carefully selected, and the parameters must be appropriately optimized so that there is a significant resolution in the sensitivity values. Because of the low on-state characteristics of TFETs, the low value of dielectric constant biomolecules proves to be more vulnerable to electronic noise. To tackle such problems, the use of current-amplifying circuits or trans-impedance amplifiers, which essentially amplify the current or convert it to an equivalent voltage, and stabilize the noise, may be a constructive option.
- The fabrication prospect of DM TFET as a biosensor is still tedious and many challenges lie in the realization of a working DM TFET biosensor, and relating the associated modeling to it. Once such works surface the research spectrum, the area shall see the light towards commercialization or at least useful inferences which may help to arrive at interesting conclusions. Therefore, to cause a major impactful shift in the technological scenario with DM TFET biosensors, the fabrication of architecture is the need of the hour.
- An altogether different outlook on DM TFETs as biosensors may be perceived through the emerging scope of use of machine learning in sensing applications. The interactions between the target and the probes, the probabilities of placement of probes, the damages to the semiconductor surface during etching of nanocavity, the biosensing circuit parameters, and the acquisition of data from biosensor arrays may be well-modeled or better predicted by machine learning algorithms.

4.2. Results for Work Done Under Objective 1

4.2.1. Nanocavity-in-Body TFET for biosensors

The key results related to the work are discussed here. The methodology has already been described in Sec. 3.2.1.

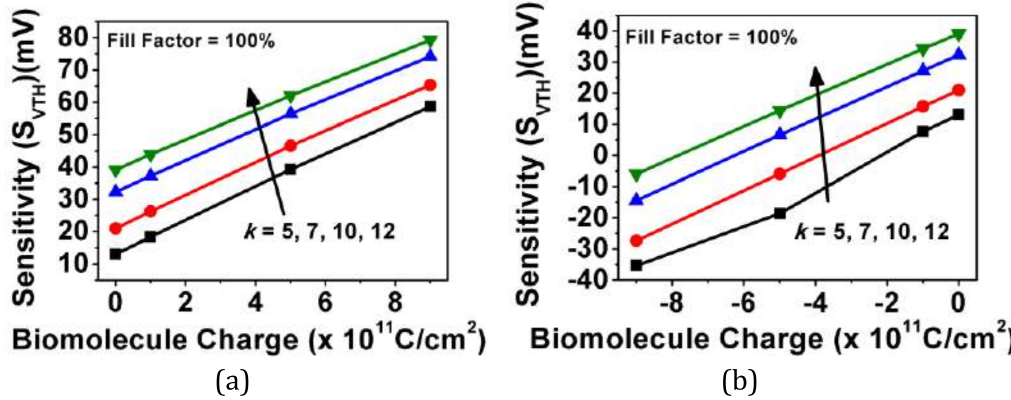
- The response of the sensor to positively charged biomolecules at the interface is higher as compared to that of negatively charged biomolecules as evident from Figure 4.2. Whereas for positively charged interface, the current sensitivity increases with the charge, for a negatively charged interface, it follows an opposite trend.



(a) (b)

Figure 4.2. Sensitivity (I_D) for (a) positive and (b) negative charge of biomolecules for different dielectric constants

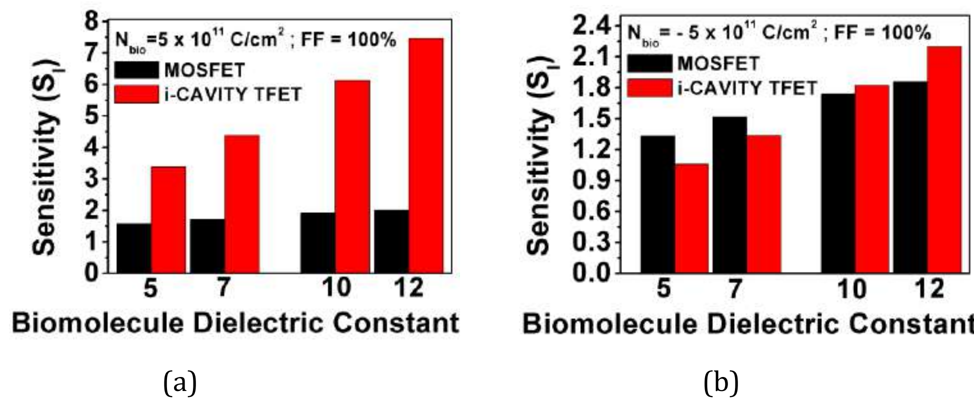
- Similar to drain current sensitivity, the threshold voltage sensitivity is an important parameter in sensing TFETs. With the increase in positive charge, the threshold voltage sensitivity increases, whereas with the increase in negative charge, the threshold voltage sensitivity decreases as shown in Figure 4.3. For negatively charged interface, the threshold voltage sensitivity possesses negative values indicating



(a) (b)

Figure 4.3. Sensitivity (V_{TH}) for (a) positive and (b) negative charge of biomolecules for different dielectric constants

- A comparison between the nanocavity-in-body TFET (i-cavity TFET) and conventional gate dielectric modulated (GDM) MOSFET as sensors are shown in Figure 4.4. For positively charged interface, the drain current sensitivity of the nanocavity-in-body TFET is better, whereas for negatively charged interface, the GDM MOSFET shows better sensitivity for lower dielectric constants; however as the dielectric constant increases, the sensitivity increases.



(a) (b)

Figure 4.4. Sensitivity comparison between MOSFET and i-Cavity TFET for (a) positive and (b) negative charge of biomolecules for different dielectric constants

- Since the band-to-band tunnelling (BTBT) rate is the primary parameter which decides the drain current in a TFET, therefore, the current sensitivity for three different cases: reference (empty or air-filled cavity), positive and negative interfaces are shown in Figure 4.5. Observing the peak BTBT rate shows the reason why the drain current sensitivity is higher for positively charged biomolecules.

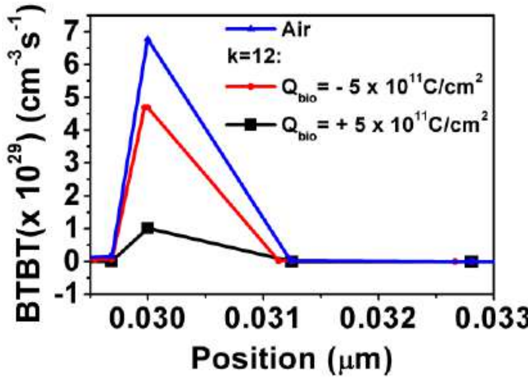
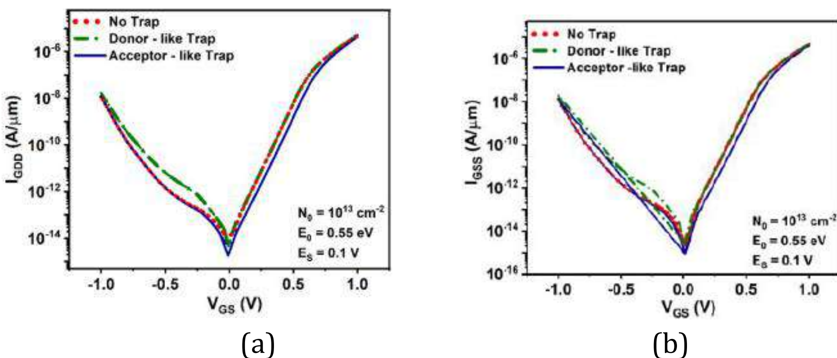


Figure 4.5. BTBT Rate for positive, negative biomolecules and air at V_{GS}=1.25 V

4.2.2. Interface trap reliability in TFETs

The key results and discussions of this work are listed here.

- Interestingly, for acceptor-like traps, the deviation of the data points from the plot with no traps is observed to significantly exist as one moves from negative gate voltages to positive gate voltages. Again, in case of donor-like traps, the deviation is observed to be significant as one moves from positive gate voltages towards negative gate voltages, signifying dominance in opposite regions of operation. It is also observed that the increase in interface trap concentration, degrades the SS value of the TFET.
- To examine the impact of traps, gate leakage currents, I_{GDD} keeping source terminal floating, and I_{GSS} keeping drain terminal floating are plotted in Figure 4.6 respectively. The characteristics for acceptor-like traps, and donor-like traps are plotted after carrying out TCAD simulations at three random source (drain) voltages for I_{GDD} (I_{GSS}) in millivolts to consider the floating terminals. The acceptor-like traps are dominant at positive V_{GS} for I_{GDD} but, in case of I_{GSS}, the trend is similar for positiveV_{GS}, but for negative V_{GS}, both donor-like, and acceptor-like traps are dominant. with the increase in temperature, keeping trap concentration constant, the on current (I_{ON}), and the off current (I_{OFF}) increase.

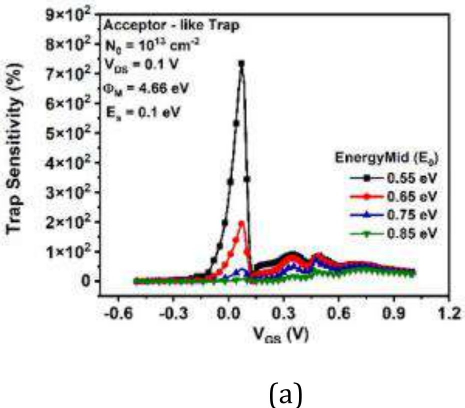


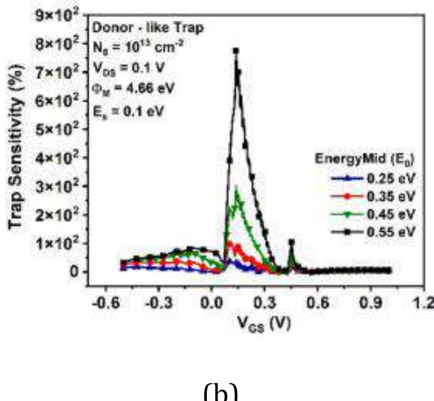
(a) (b)

Figure 4.6. (a) I_{GDD} keeping source terminal floating, (b) I_{GSS} keeping drain terminal floating.

- The effect of Gaussian peak location on trap sensitivity is shown in Figure 4.7 where it was found that the peaks of the trap sensitivity have a decreasing trend for both acceptor-like, and donor-like traps. This suggests that the location of the peak of the

Gaussian trap distribution away from the band edges results in higher degrees of sensitivity.

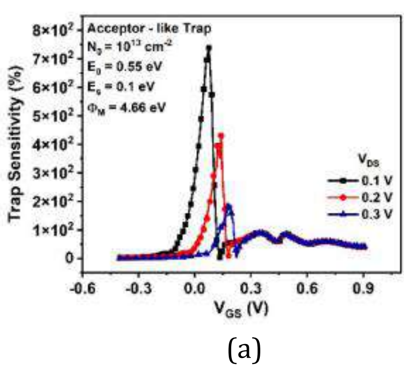


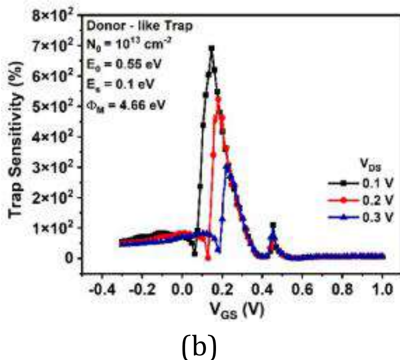


(a) (b)

Figure 4.7. (a) Trap Sensitivity for energy mid for acceptor-like trap; (b) Trap Sensitivity for energy mid for donor-like traps.

- Figure 4.8 shows the effect of drain voltage on trap sensitivity where observations are made as follows: as we increase the drain voltage V_{DS} for n-type TFET, the ambipolar current increases, which indicates greater tunneling of carriers in the channel-drain junction. As the acceptor like trap is more dominant at the junction than donor-like trap so as the drain voltage increases, the peak sensitivity increases accordingly shown in Figure 4.8.





(a) (b)

Figure 4.8. (a) Trap Sensitivity for drain voltage for acceptor-like traps; (b) Trap Sensitivity for drain voltage for donor-like traps.

- Figure 4.9 shows the effect of gate–drain underlap on trap sensitivity where the peaks in trap sensitivity lie in the region of transition from ambipolar region to subthreshold region of operation, where the percentage change in values of drain current is high. Although the peak position of the trap sensitivity seems to shift towards left as one increases the gate–drain underlap length, there is a conflict in this trend between the cases for $L_{UN} = 20nm$, and $L_{UN} = 30nm$ shown in Figure 4.9.

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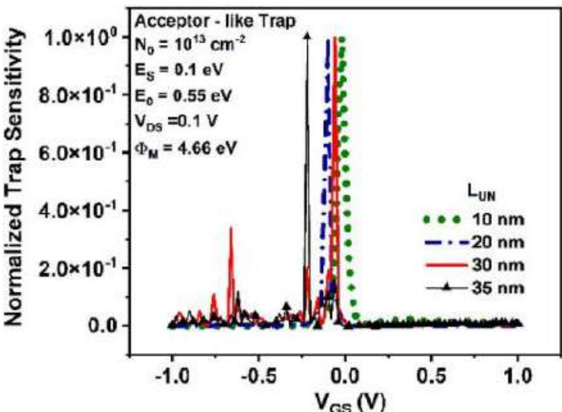
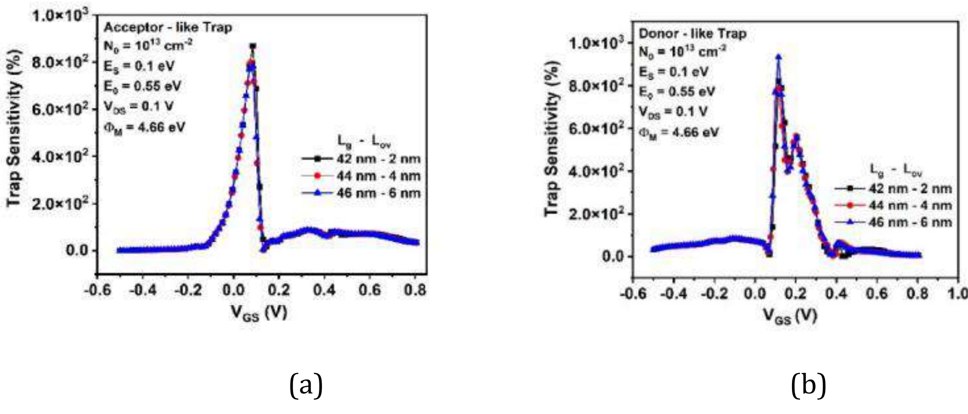


Figure 4.9. Trap Sensitivity for gate–drain underlap for acceptor-like traps.

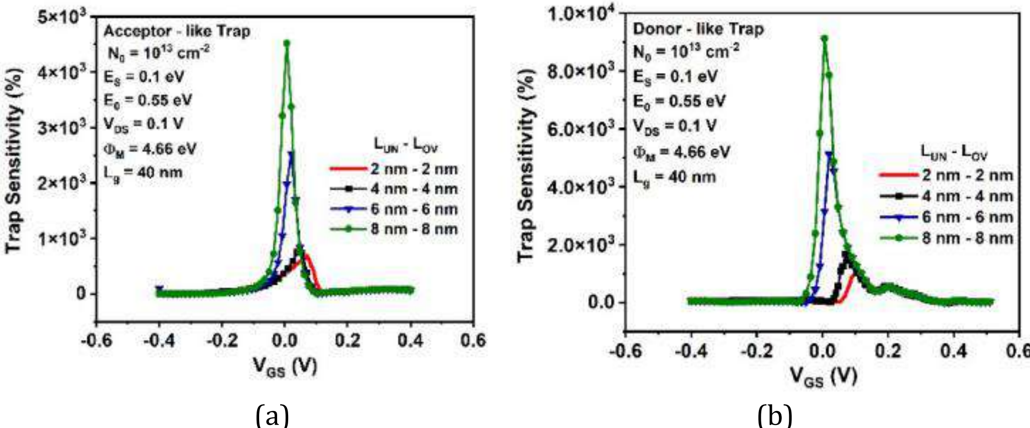
- Figure 4.10 depicts the effect of gate–source overlap on trap sensitivity. Throughout the change of gate–source overlap lengths, a gate–drain underlap length of 0 nm is maintained. The values for peak sensitivity for both acceptor-like traps and donor-like traps as the gate length is increased shown in Figure 4.10. With the increase in L_{OV}, the position of band-bending of bands near the junction shifts towards the source region, thereby increasing the BTBT area. The maximum band bending occurs at a gate–source overlap of 4 nm i.e., towards left of source -channel junction, resulting in higher current.



(a) (b)

Figure 4.10. (a) Trap Sensitivity for gate–source overlap for acceptor-like traps; (b) Trap Sensitivity for gate–source overlap for donor-like traps.

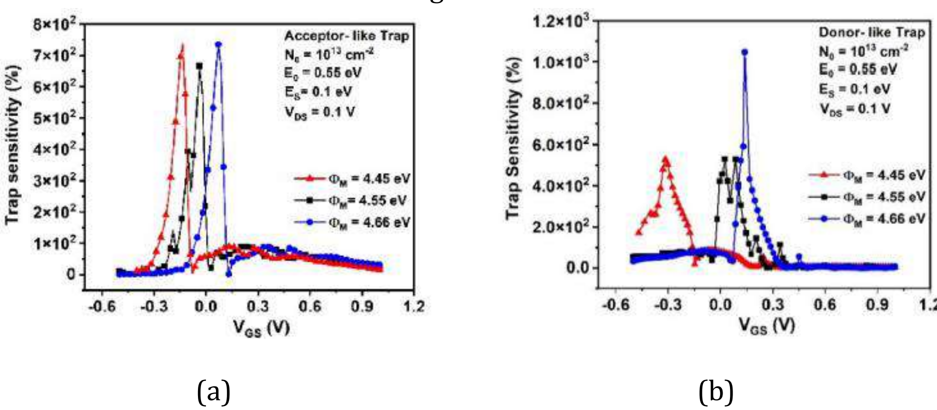
- Regarding the effect of simultaneous gate–source overlap and gate–drain underlap on trap sensitivity in the conventional $p-i-n$ SOI $TFET$, the gate–drain underlap (L_{UN}) plays an important role in ambipolarity, and the gate– source overlap (L_{OV}) increases the on current. Therefore, in this section, the gate lengths are varied by equal, and simultaneous increase in gate–drain underlap length, and gate–source overlap length so that the gate length stays constant at 40 nm. Figure 4.11 shows that with an increase in L_{UN} = L_{OV}, the position of peak sensitivity shifts towards the left.



(a) (b)

Figure 4.11. Trap Sensitivity for gate–source overlap and gate–drain underlap for (a) acceptor-like traps; (b) donor-like traps.

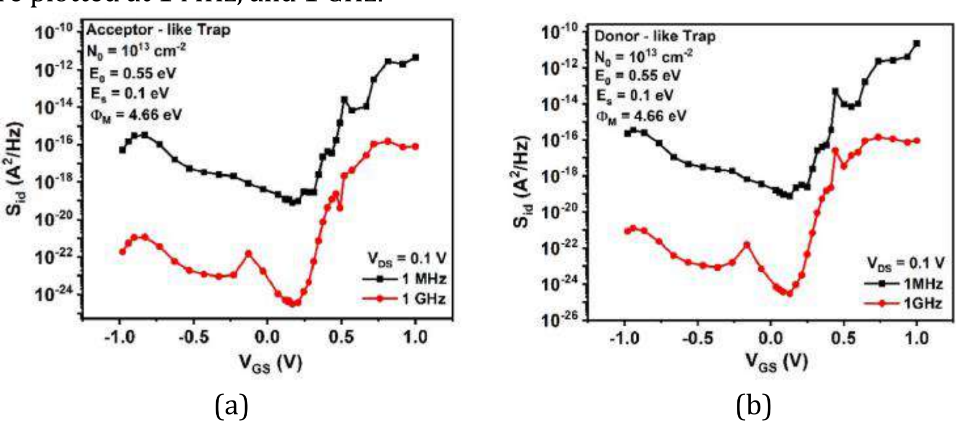
- Figure 4.12 shows the effect of gate work-function on trap sensitivity. Here the peaks of the trap sensitivity are found to shift towards the left with the decrease in work-function as evident from Figure 4.12. indicating the shift of the transfer characteristics towards the left due to the reduction in flat-band voltage.



(a) (b)

Figure 4.12. Trap Sensitivity for gate work-function for (a) acceptor-like traps; (b) donor-like traps.

- Effect of interface traps on noise spectral densities is shown in Figure 4.13 where the drain current noise spectral densities (S_{id}) for acceptor-like, and donor-like interface traps are plotted at 1 MHz, and 1 GHz.



(a) (b)

Figure 4.13. Drain current noise spectral density at frequencies of 1 MHz and 1 GHz for (a) acceptor-like, and (b) donor-like interface traps

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- At a higher frequency, S_{id} is less due to its inverse dependence on frequency. The values are found to follow the drain current plot because of the direct dependence of S_{id} on it. The net gate voltage noise spectral density (S_{vg}) is related to S_{id} through g_m^2 as evident from Figures 4.14 (a) and (b). Figures 4.14 (c) and (d) offer information on the contribution of each noise source at 1 MHz the monopolar generation-recombination noise is dominant at this frequency. Flicker noise has higher values than diffusion noise for negative V_{GS} whereas in the on-state, both are similar. However, at a higher frequency of 1 GHz, the diffusion noise is dominant in the on-state, whereas, flicker noise is suppressed show in figure.

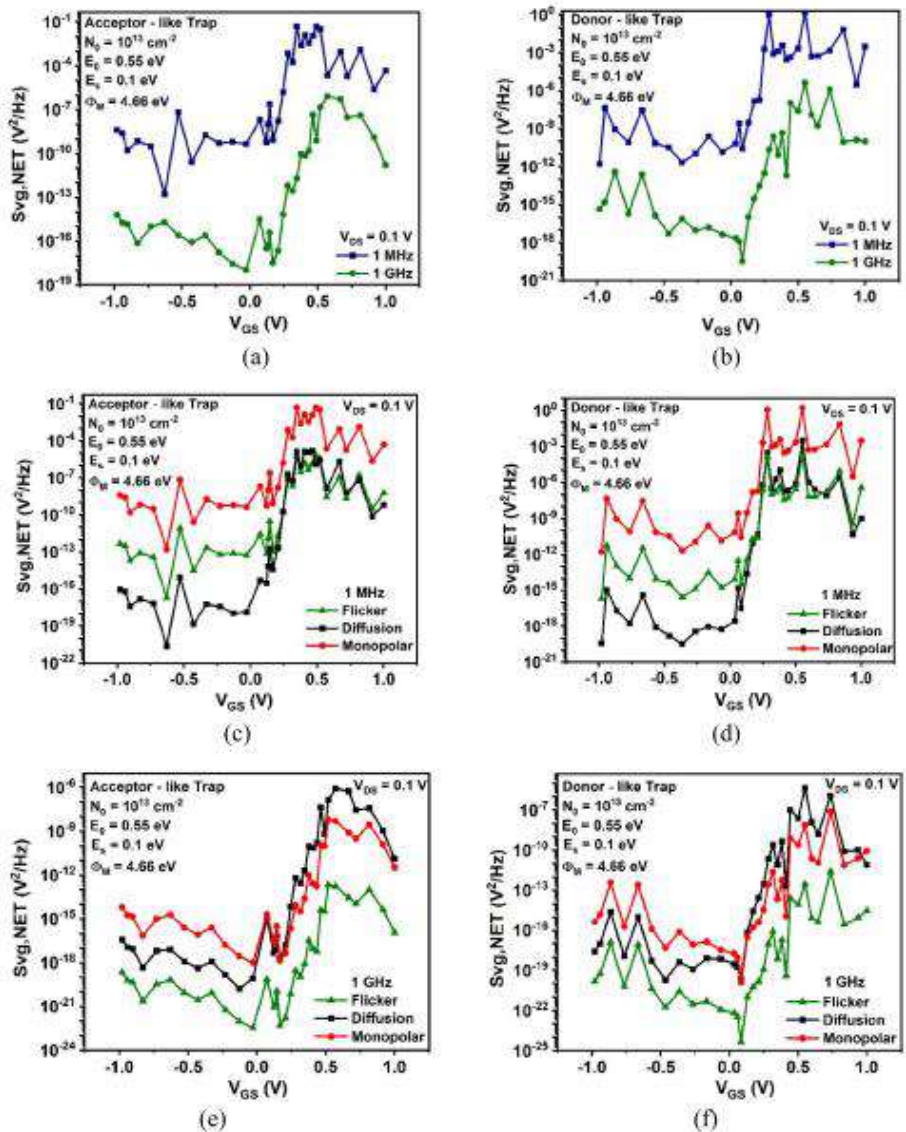

Figure 4.14. Net gate voltage noise spectral density at frequencies of 1 MHz and 1 GHz for (a) acceptor-like interface traps, and (b) donor-like interface traps; Gate voltage noise spectral densities in presence of flicker, diffusion, monopolar G-R noise sources for (c) acceptor-like interface traps (1 MHz), (d) donor-like interface traps (1 MHz), (e) acceptor-like interface traps (1 GHz), (f) donor-like interface traps (1 GHz).

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4.2.3. Alternative TFET geometries

(a) Double Gate n-p-n TFET

This section represents the key results from the methodology of the work described in Sec. 3.2.3 (a).

- Because the junction depletion width for reduced drain doping is wide and reduces the tunnelling likelihood on application of negative gate-to-source voltages (V_{GS}), the ambipolar current decreases as the concentration of the drain dopant decreases which is shown in Figure 4.15.

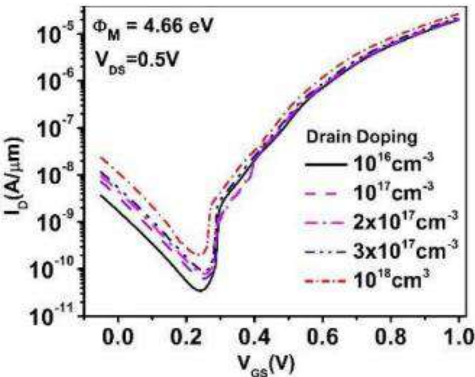


Figure 4.15. Transfer characteristics for different drain doping concentration

- Transfer characteristics for various gate-on-drain lengths (L_{GD}) are shown in Figure 4.16, taking the optimised N_{Drain} from the preceding phase into account. Because the influence of the gate on the drain energy bands is reduced with a decrease in L_{GD}, the ambipolar current also decreases shown in Figure 4.16.

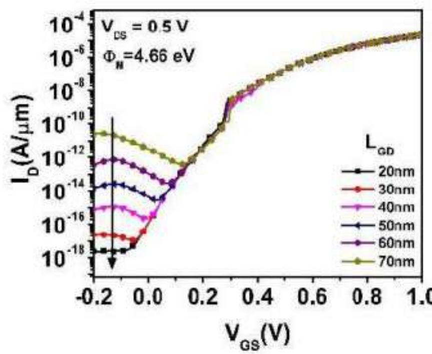


Figure 4.16. Transfer characteristics for different gate-on-drain lengths

- For work function variation, see the following section. The transfer characteristics for various gate metal workfunctions (φ_M) are shown in Figure 4.17 while considering the optimised values of N_{Drain} and L_{GD} from earlier steps. With an increase in φ_M the graphs move to the right, resulting in greater threshold voltage (V_{TH}) and lower I_{ON}. Further parameter optimization is thought to be possible with an optimised value of 4.66 eV.

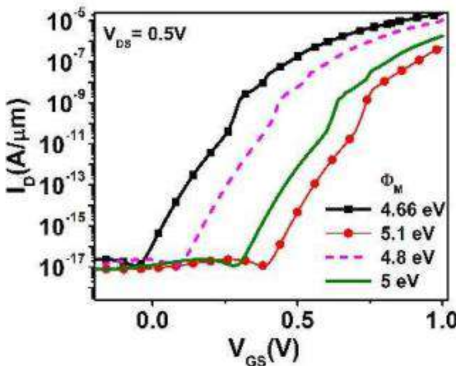
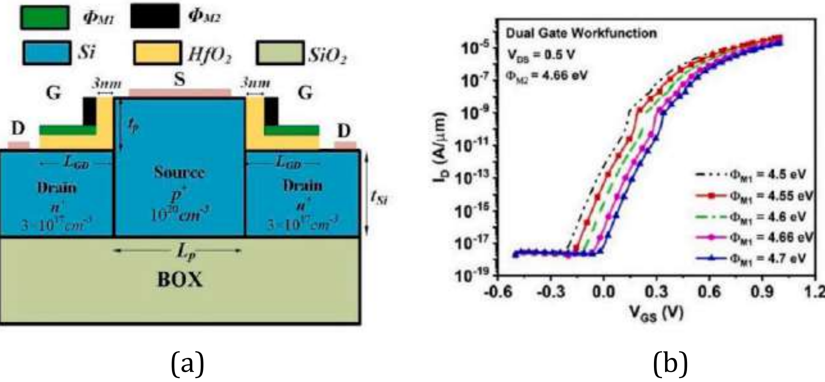


Figure. 4.17. Transfer characteristics for different gate metal workfunction

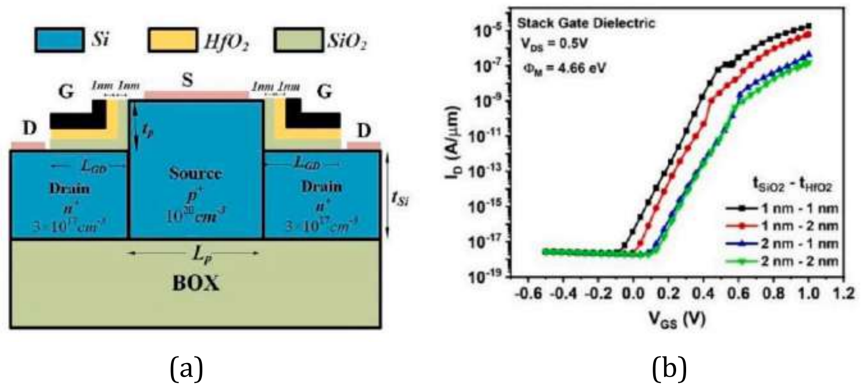
- The dual gate dielectric, stack gate dielectric, and dual gate work function strategies are implemented, and the three TFETs are investigated, and compared for optimum electrical parameters which are shown in the figure below.



(a) (b)

Figure 4.18. (a) Architecture of the dual gate work function n-p-n SOI DG TFET, (b) Transfer characteristics for different work functions of the lateral gate placed over drain (Φ_{M1}).

- The architecture for dual gate work function n-p-n SOI DG TFET is shown in Figure 4.18 (a) where two different work functions are used for the lateral, and vertical gate structures. The work function of the lateral gate which is placed over the drain, φ_{M1}, is varied for optimization. As evident from the dependence of the transfer characteristics on the work function, the curve shifts to the right when φ_{M1} increases.



(a) (b)

Figure 4.19. (a) Architecture of the stack gate dielectric n-p-n SOI DG TFET, (b) Transfer characteristics for different thickness of the two gate oxides.

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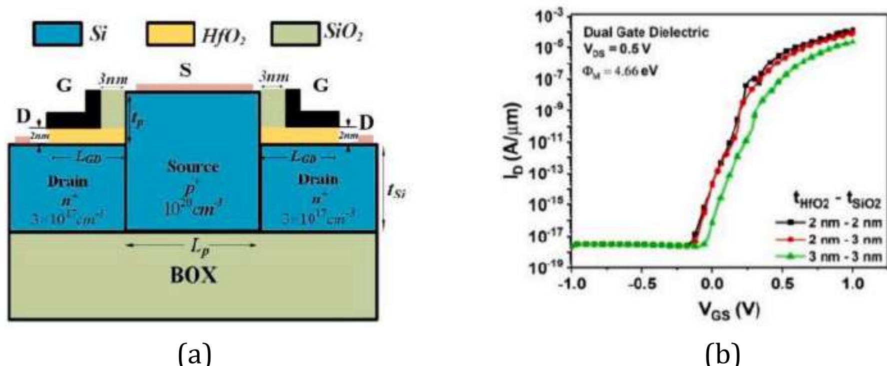
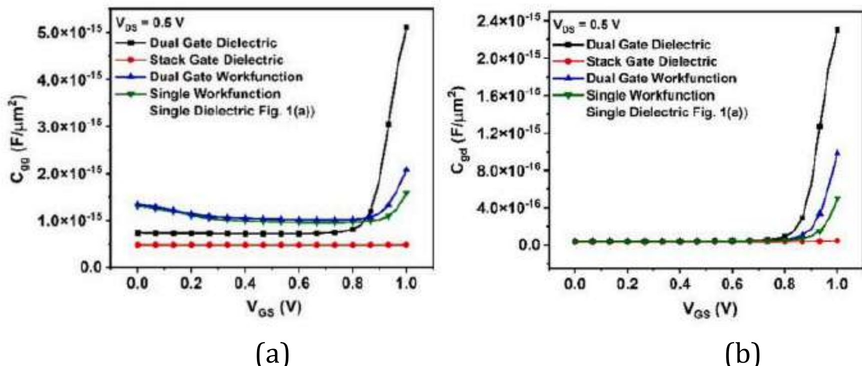
- Fig. 4.19 (a) represents the stack gate dielectric n-p-n SOI DG TFET where the two gate oxides are stacked over one another. A variation of the oxide thickness of the two oxides, t_{SiO_2} for SiO_2, and t_{HfO_2} for HfO_2, is carried out, and the transfer characteristics are shown in Figure 4.19 (b). A lower gate dielectric thickness corresponds to a higher drain current.



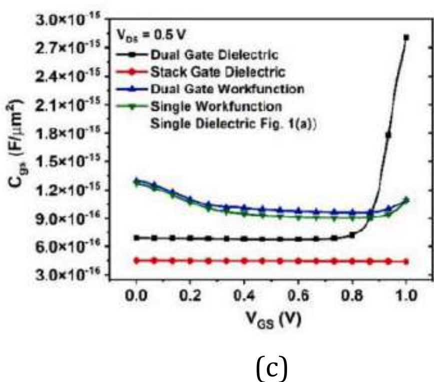
(a) (b)

Figure 4.20. (a) Architecture of the dual gate dielectric n-p-n SOI DG TFET; (b) Transfer characteristics for different thickness of the two gate oxides;

- Figure 4.20 (a) depicts the architecture of the dual gate dielectric n-p-n SOI DG TFET where the high-k gate dielectric covers the drain, and the low-k dielectric covers the remaining portion of the source. The transfer characteristics for different thickness of the two gate oxides are shown in Figure 4.20 (b). For a lower gate dielectric thickness of 2 nm, the drain current is higher but the presence of a hump-like feature in the curve due to which this must be discarded. On the other hand, increasing the vertical gate dielectric (on source) thickness (t_{SiO_2}) to 3 nm reduces this undesirable feature. Although the on currapplicationsred, yet the change is not significant, and hence, t_{SiO_2} = 3nm is recommended for low power applicatns. The DIBL values ($V_{TH1} - V_{TH2}/V_{DS1} - V_{DS2}$) for the four architectures were found, and the values of V_{DS} taken are 50 mV and 0.5 V and V_{TH} is the threshold voltage. For the constant current method, the DIBL is extremely low, and negative for three architectures.
- Three capacitances, C_{gg}, C_{gs}, and C_{gd}, are plotted versus V_{GS} for four geometries in Figure 4.21 in which the dual gate dielectric SOI DG n-p-n TFET exhibits the highest capacitance values, whereas the stack gate counterpart exhibits lowest values of capacitance

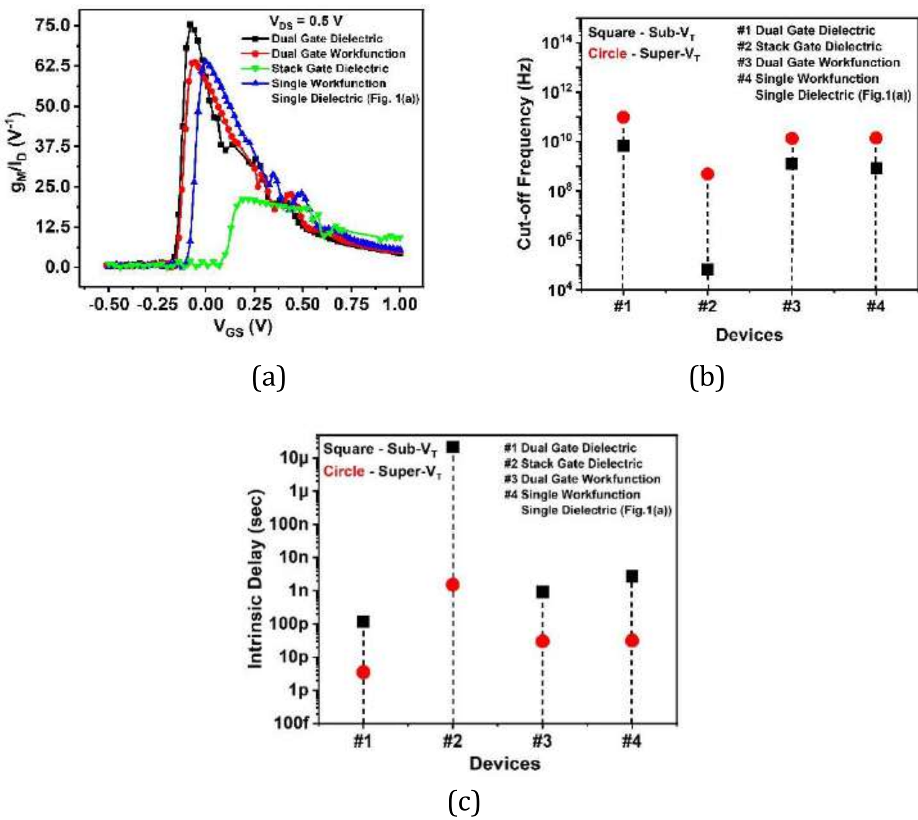


(a) (b)



(c)

Figure 4.21. Plot of (a) total gate capacitance, (b) gate-to-drain capacitance, (c) gate-to-source capacitance versus V_{GS}



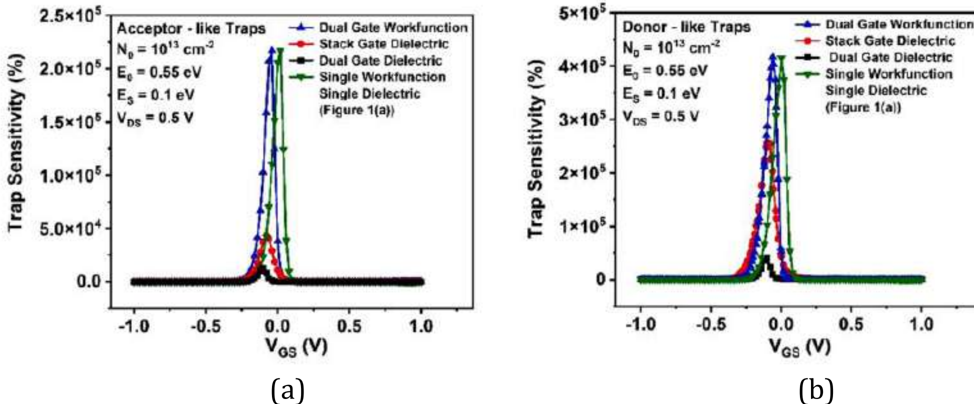
(c)

Figure 4.22. (a) Transconductance efficiency versus V_{GS}; (b) Cut-off frequency in subthreshold and superthreshold regions for four proposed architectures

- Analysis for subthreshold circuit application in terms of transconductance efficiency gm/ID, cut-off frequency, and intrinsic gate delay is plotted in Figure 4.22. Due to the superior transfer characteristics of the dual gate dielectric SOI DG n-p-n TFET, the transconductance efficiency has the highest peak, and steepest slope than the other architectures as shown in Figure 4.22 (a). The cut-off frequency is given by $f_T = g_m/2\pi C_{gg}$ and is plotted for subthreshold as well as superthreshold regimes in Figure 4.22 (b) to have a distinct observation. For the dual gate dielectric geometry, the cut-off frequency is the best, and the difference between the frequencies in subthreshold and superthreshold regimes is less, indicating a consistent behavior. The intrinsic gate delay, τ, is plotted in Figure 4.22 (c) using the relation $\tau = C_{gg} V_{DD}/I_D$, where, $V_{DD} = V_{DS}$ and I_D is the drain

current. Two values of τ are plotted for the four architectures, one in the subthreshold regime, and the other in the superthreshold regime of operation. The stack gate dielectric geometry is slower than the dual gate dielectric geometry.

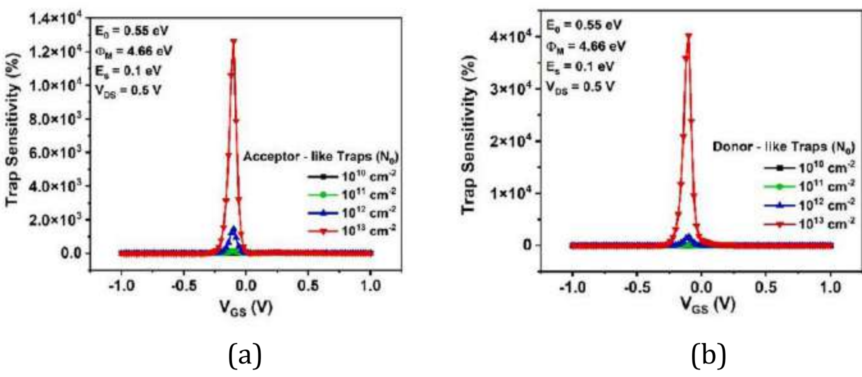
- Comparing the interface traps of all three geometries it is observed that the dual gate dielectric n-p-n SOI DG TFET has the lowest trap sensitivity (Figure 4.23).



(a) (b)

Figure 4.23. Trap sensitivity versus gate-to-source voltage for four proposed architectures of *n-p-n* SOI DG TFET for (a) acceptor-like traps, (b) donor-like traps

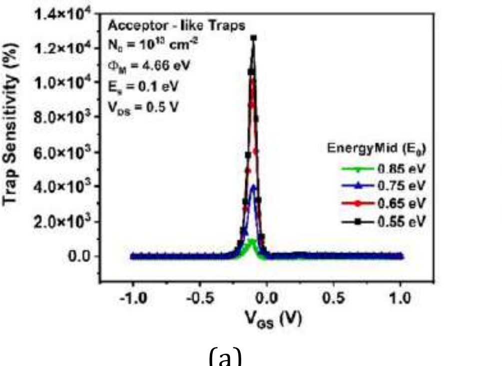
- The maximum peak percentage sensitivity for acceptor-like traps is 12615.44% at V_{GS} = -0.1 V for 10^{13} cm^{-3} concentration. Similarly, the maximum peak percentage sensitivity for donor-like traps is 40226.91% at V_{GS} = -0.1 V for 10^{13} cm^{-3} concentration (Figure 4.24).

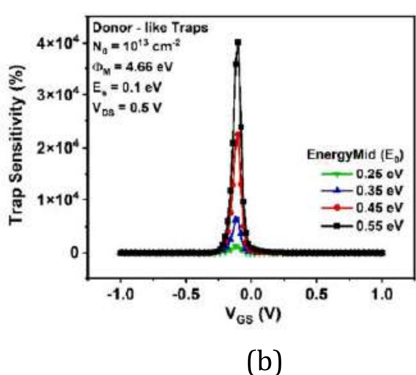


(a) (b)

Figure 4.24. Trap sensitivity versus gate-to-source voltage for different peak concentrations in dual dielectric *n-p-n* SOI DG TFET for **(a)** acceptor-like traps, **(b)** donor-like traps

- The location of the trap level is varied both for acceptor-like trap and donor-like traps where it is observed that the percentage peak sensitivity of acceptor-like traps and donor-like traps is 12615.44% and 40226.91% in the deep level traps (Figure 4.25), and the percentage gradually decreases as the trap moves towards the shallow level.

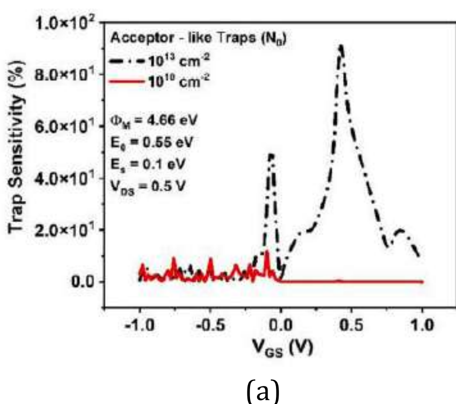


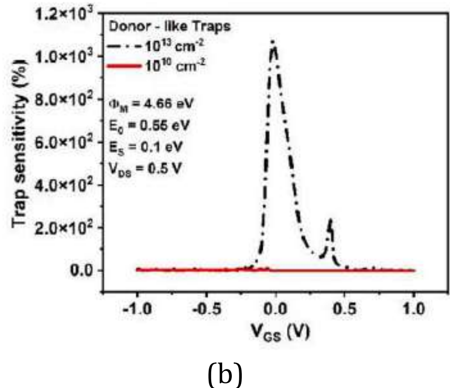


(a) (b)

Figure 4.25. Trap sensitivity versus gate-to-source voltage for different values of E_0 in dual dielectric *n-p-n* SOI DG TFET for (a) acceptor-like traps, (b) donor-like traps

- In TFETs, the band-to-band tunneling region near the junction close to the surface is the most sensitive. Scaling down the gate length aggressively to 5 nm within the band-to-band tunneling region, the peaks of trap sensitivity for acceptor-like as well as donor-like traps interestingly change as shown in Figure 4.26. This indicates that the gate length plays a major role in determining the position of trap sensitivity for interface traps in TFETs.

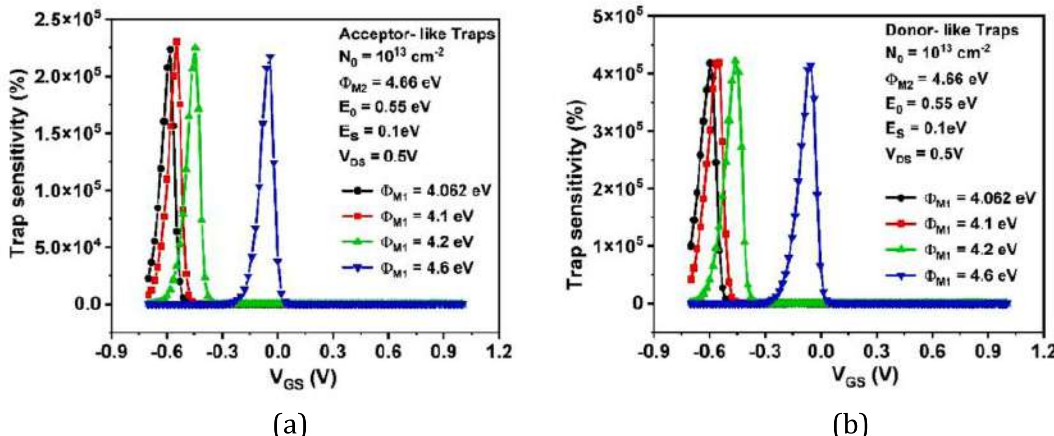




(a) (b)

Figure 4.26. Trap sensitivity versus V_{GS} in dual gate dielectric SOI DG *n-p-n* TFET for (a) acceptor-like traps and (b) donor-like traps

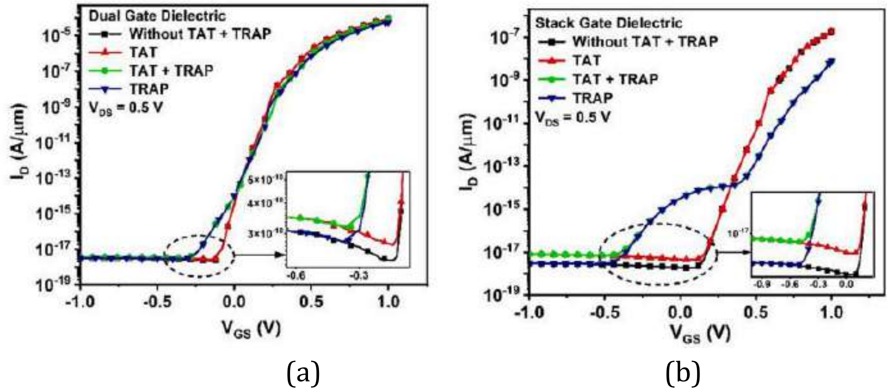
- Although the role of the gate in controlling channel potential is an established phenomenon still, an additional experiment was carried out to ascertain the dependence of peak of trap sensitivity on gate properties by varying the work function in dual gate work function TFET. The peaks are found to shift towards the left with the decrease in work function as evident from Figure 4.27, indicating the shift of the transfer characteristics towards the left due to the reduction in flat band voltage.



(a) (b)

Figure 4.27. Trap sensitivity versus V_{GS} in dual gate work function SOI DG *n-p-n* TFET for (a) acceptor-like traps and (b) donor-like traps

- The effect of trap-assisted tunneling (TAT) on drain current depending on the dominance of either the BTBT rate or the TAT rate is anaylzed. For this, four different cases have been taken: (a) without TAT or interface traps, (b) only TAT, (c) only interface traps, and (d) with both TAT and interface traps. comparing both (a) and (b) the drain current increases in (b) in the ambipolar region.
- From Figures 4.28 (a) and (b), comparing the TAT cases, and the non-TAT cases, the current in the former is slightly higher than that in the latter because the addition of a trap level enhances the carrier tunneling between bands even in the off-state, and ambipolar region. However, the difference is low because the BTBT rate is higher than the TAT (SRH) rates at the calibrated values of the device. This suggests that in a TFET with a BTBT rate comparable to TAT (SRH) rate, the difference in drain current shall be prominent. One way to have reduced the BTBT rate at the tunnel junction is through an increased gate dielectric thickness. Therefore, in the case of stack gate dielectric SOI n-p-n DG TFETs where the overall gate dielectric thickness is 4 nm, the difference between TAT and non-TAT cases is more significant than the dual dielectric SOI n-p-n DG TFET where the gate dielectric thickness is 2 nm.



(a) (b)

Figure 4.28. Transfer characteristics of (a) dual gate dielectric *n-p-n* SOI DG TFET, and (b) stack gate dielectric *n-p-n* SOI DG TFET

(b) *Junctionless TFET*

This section represents the key results from the methodology of the work described in Sec. 3.2.3 (b).

- In the case of temperature variation, it is observed that the ON-current of the $p-i-n\ SOI\ TFET$ increases more with temperature than JL-TFET.
- It is observed that the OFF-current of the JL-TFET is less increased with temperature than $p-i-n\ SOI\ TFET$ and therefore JLTFET has better (I_{ON}/I_{OFF}) ratio then $p-i-n\ SOI\ TFET$.
- The threshold voltage (V_{TH}) for both devices decreases at higher temperatures which are shown in the Figure 4.29 below

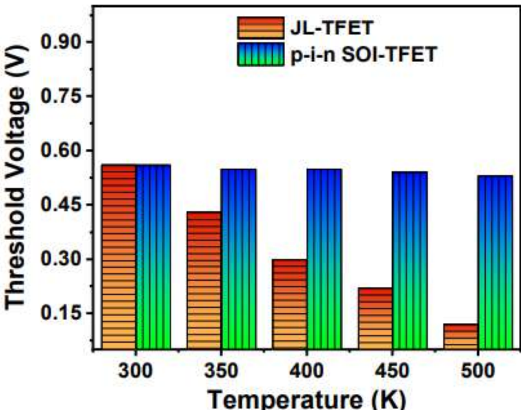


Figure 4.29. Bar diagram of threshold voltage of both the device.

- As transconductance is a significant metric for analog circuit design it describes how well the amplification can be performed for circuit applications. So, from the study, it is concluded that the transconductance of JL-TFET increases with temperature as in the conventional TFET shown in the Figure 4.30.

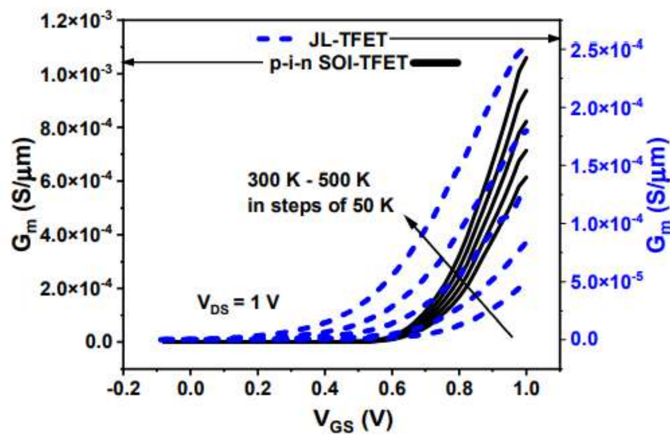


Figure 4.30. The transconductance curve of both JL-TFET and Conventional TFET.

- For better performance of the device, the total gate capacitance C_{GG} of the device must be less, which affects the cut-off frequency of the device shown in Figure 4.31.

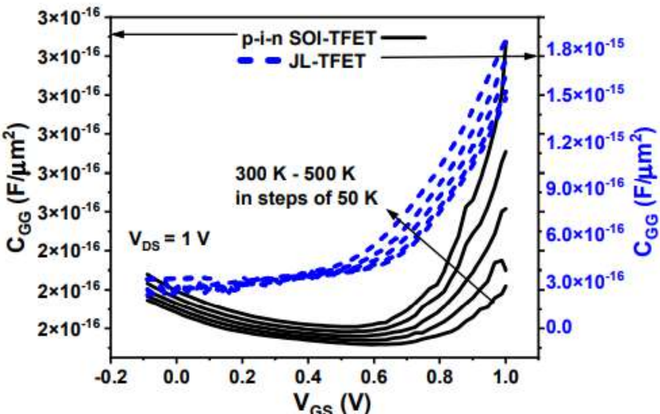


Figure 4.31. The total gate capacitance curve of both JL-TFET and Conventional TFET.

- Study of cut-off frequency is also done which is a function of C_{GS} and C_{GD}, which are also dependent on temperature. The cut-off frequency for both the devices for temperature variation is shown in Figure 4.32.

$$f_T = {G_m}/{2\pi(C_{GS} + C_{GD})} = {G_m}/{2\pi C_{GG}} \tag{4.1}$$

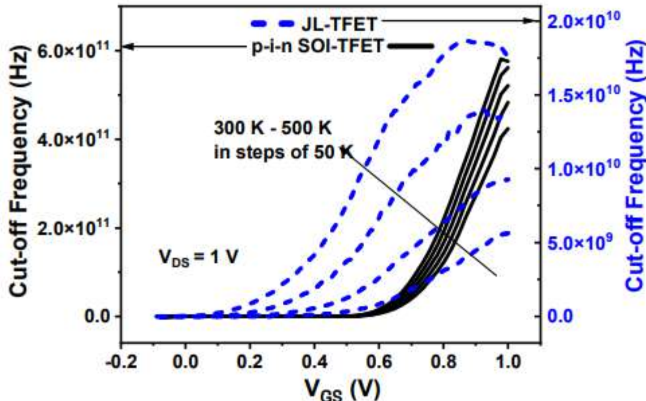


Figure 4.32. Cut-off frequency vs gate voltage (V_{GS}) curve of both JL-TFET and Conventional TFET.

- It is observed from the GBW product that maximum values of 2.8 MHz and 2.1 GHz are observed for JL-TFET and p-i-n TFET respectively as seen in Figure 4.33. It is observed that p-i-n SOI TFET has improved GBP, both at room temperature and higher temperature, making the device suitable for analog applications and higher temperature.

$$GBW = {G_m}/_{2\pi} \times 10 \times C_{GD} \tag{4.2}$$

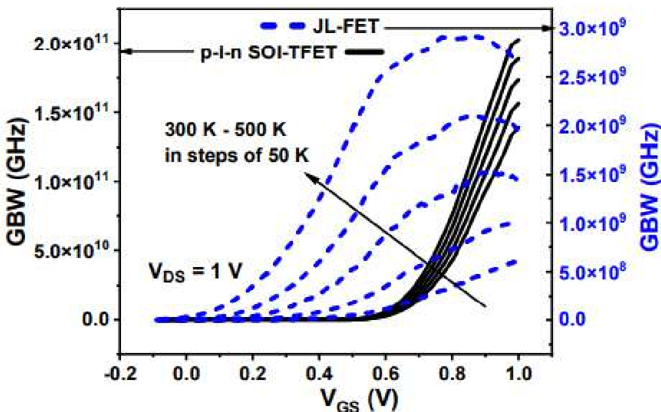


Figure 4.33. The gain bandwidth product vs gate voltage (V_{GS}) curve for both JL-TFET and Conventional TFET.

4.3. Results for Work Done Under Objective 2

A comparison of partial hybridization (PH) is done between the nanocavity-in-body TFET sensor and a TFT sensor (*refer to Sec. 4.3 for methodology*). The key results are discussed here.

- The nanocavity-in-body TFET sensor under PH condition, shows drain current sensitivity as shown in Figure 4.34. For negatively charged biomolecules, the sensitivity is low as compared to that for positively charged biomolecules.

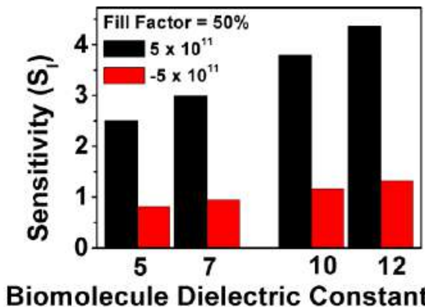
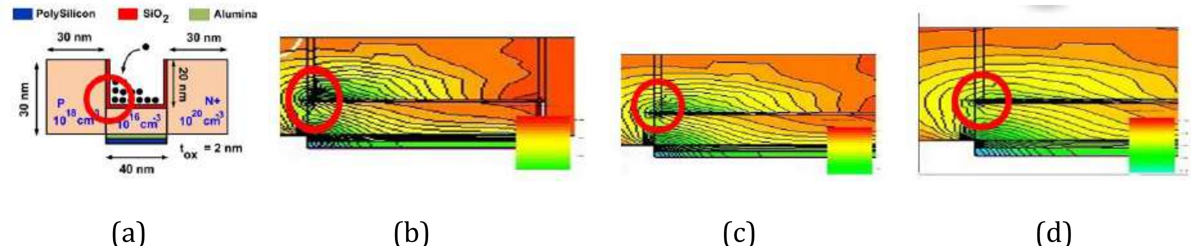


Figure 4.34. Sensitivities for FF = 50%

- Important information is revealed regarding the presence of a backtrack electric field around the body cavity as shown in Figure 4.35. The electric field is higher for dielectric constant, k = 1 and decreases. This is an important characteristic of the nanocavity-in-body TFET, and is an interesting result which has not yet been revealed.



(a) (b) (c) (d)

Figure 4.35. (a) Location in the device showing the point of interest. Contour of electric field at the semiconductor-biomolecule interface for (b) k = 1; (c) k = 2.1; (d) k = 4;

- Two FFs of ~46% and ~71% are considered here for both the profiles. Figure 4.36 shows the drain current sensitivity for the two profiles for a value of negative charge, $Q_{bio} = -10^{11}qcm^{-2}$ and a value of positive charge, $Q_{bio} = +10^{11}qcm^{-2}$. The decreasing profile exhibits a slightly higher sensitivity value than the increasing profile. For $Q_{bio} = -10^{11}qcm^{-2}$, the sensitivity values are low as compared to its positive counterpart. However, the percentage change in sensitivity when one moves from streptavidin to protein for a specific profile is higher for the negatively charged molecules than the positively charged ones.

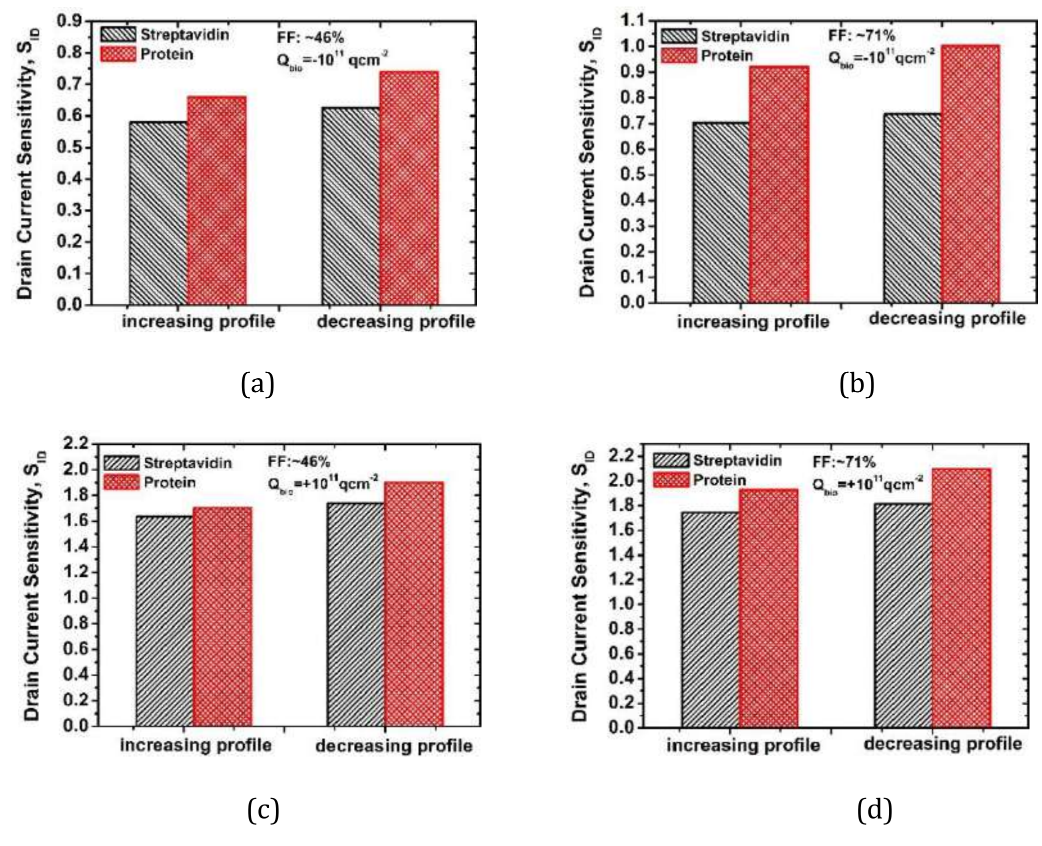


Figure 4.36. Drain current sensitivity for two biomolecule profiles for (a) FF ~46%, $Q_{bio} = -10^{11}qcm^{-2}$; (b) FF ~71%, $Q_{bio} = -10^{11}qcm^{-2}$; (c) FF ~46%, $Q_{bio} = +10^{11}qcm^{-2}$; (d) FF ~71%, $Q_{bio} = +10^{11}qcm^{-2}$

- Figure 4.37 plots the threshold voltage sensitivity for two FFs as in Figure 4.36. For positively charged biomolecules in Figure 4.37 (c) and Figure 4.37 (d), the response of the sensor is

significant in terms of percentage change while one moves from streptavidin to protein. Similarly, the percentage change in sensitivity is more pronounced while moving from one profile to another. This is not observed in the case for negatively charged biomolecules in Figure 4.37 (a) and Figure 4.37 (b). For decreasing profile in these figures, the value for protein is slightly lower than that of streptavidin.

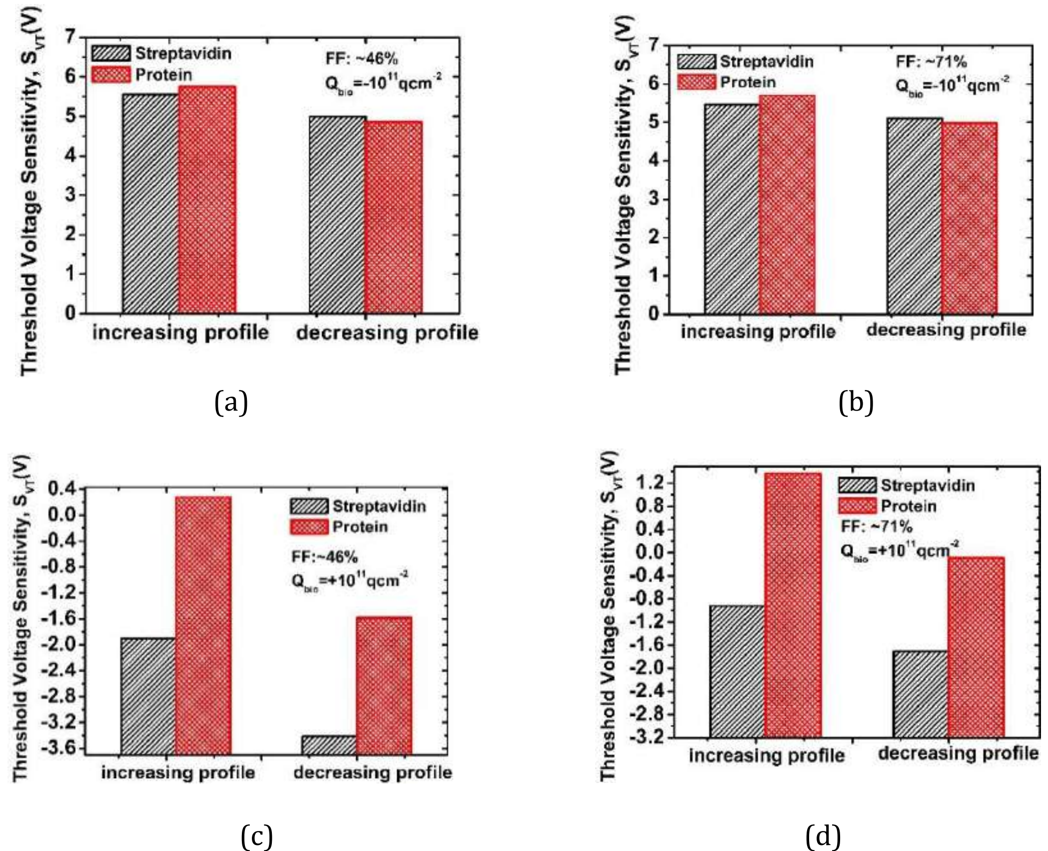


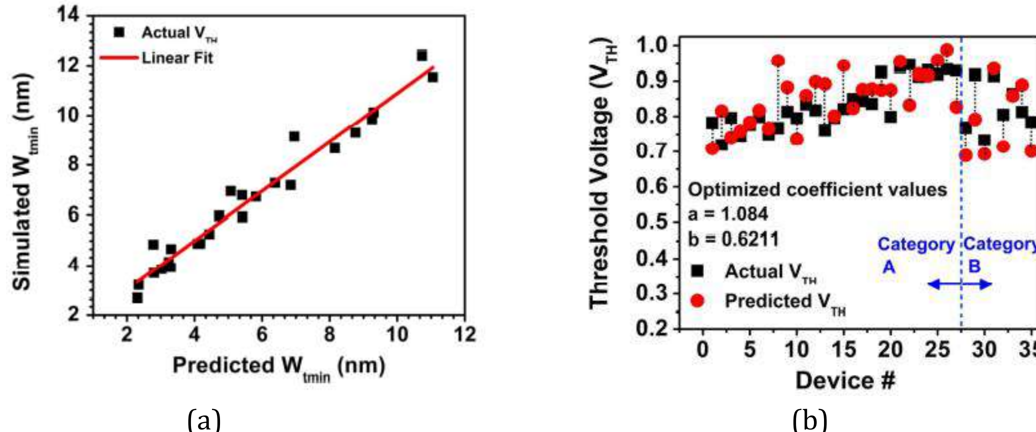
Figure 4.37. Threshold voltage sensitivity for two biomolecule profiles for (a) FF ~46%, $Q_{bio} = -10^{11}qcm^{-2}$; (b) FF ~71%, $Q_{bio} = -10^{11}qcm^{-2}$; (c) FF ~46%, $Q_{bio} = +10^{11}qcm^{-2}$; (d) FF ~71%, $Q_{bio} = +10^{11}qcm^{-2}$

4.4. Results for Work Done Under Objective 3

4.4.1. Threshold Voltage Extraction Model

The key results for the work are discussed here.

- Based on the theory and the algorithm presented in Sec. 3.4.1, the results for the model are shown in Figure 4.38 (a) shows the linear relationship between the simulated and predicted W_{tmin} values for the set of 27 devices belonging to category A, thus establishing that the linear regression technique fits the prediction.
- Apart from the 27 known devices for Category A, 8 devices for Category B were taken, and the model was extended to predict their threshold voltages as well (Figure 4.38 (b)).



(a) (b)

Figure 4.38. (a) Predicted versus simulated $W_{tmin}(R^2 = 9.5\%)$; (b) Plots of the actual versus predicted V_{TH} values for category A as well as category B.

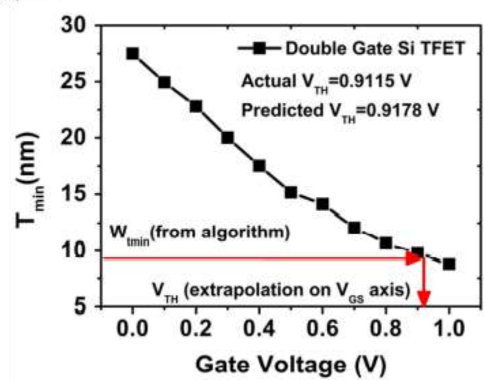


Figure 4.39. Mapping of W_{tmin} to V_{TH} achieved using the simple extrapolation.

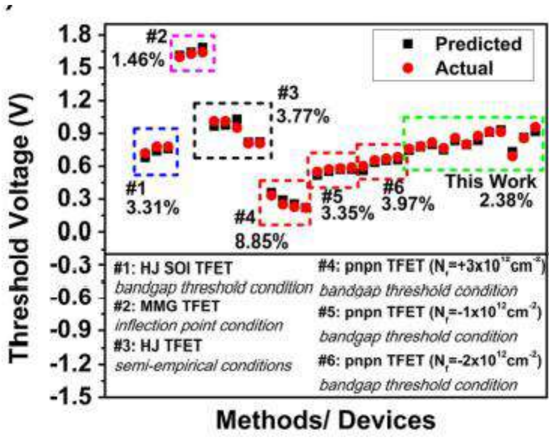


Figure 4.40. Six different cases of application of reported threshold voltage models for TFETs are plotted, showing their sets of actual (simulated) and modeled (predicted) values, as well as the average error percentage between them.

- The proposed model is dependent on the tunneling width (Figure 4.39), which makes it robust and immune to the type of conduction, as the drain current in both cases is a function of the tunneling width. The inherent relationship between the threshold voltage of each TFET and its tunneling width is universally true irrespective of the different, nonideal or complex processes occurring.

- The error percentage for around 80% of the sample devices taken in this work comes to 4.87% (Figure 4.40), which is significantly good considering the different types of devices used in the model.

4.4.2. A Figure of Merit for Low Power Devices

Using the methodology described in Sec. 3.4.2, the figure-of-merit expression is tabulated in Table 4.1. The importance of this work lies in the design of a quantitative method to determine the performance of a FET through a single numerical value. When a FET is used as a sensor as described in the project, the same parameters hold true; therefore, the FOM can be used as a universal expression for determining the overall performance of a FET.

Table 4.1. Calculation of FOM for different low power devices.

Architecture	I_{ON} (μA μm^{-1})	I_{ON}/I_{OFF}	V_{th} (V)	SS (mV dec^{-1})	I_{AMBI} (A μm^{-1})	FOM
LONG CHANNEL N-TFET [15]	12.10	2.24×10^{3}	0.12	52.8	2.01×10^{-10}	21.40
GATED PN TFET [16]	0.147	3.57×10^{10}	0.18	31.8	1.78×10^{-14}	18.10
Ge source vTFET [17]	27.60	1.16×10^{11}	0.20	21.20	1.20×10^{-14}	60.50
ED-TFET [18]	0.214	4.77×10^{7}	0.9	50.1	9.30×10^{-12}	3.71
GU-ED-TFET [18]	0.221	1.38×10^{8}	0.9	49.6	9.20×10^{-19}	4.18
TM-GU-ED-TFET [18]	14.0	8.75×10^{9}	0.64	36.1	9.20×10^{-19}	34.20
CG-TFET [19]	27.11	2.14×10^{7}	0.792	57.02	1.00×10^{-17}	26.10
GOSC TFET [20]	37.5	2.78×10^{8}	0.6	65	3.67×10^{-17}	31.30
THIN BODY-HFO_2-TFET [21]	0.011	2.65×10^{5}	2.3	330	1.50×10^{-13}	2.99
DS-TFET [22]	2.5	1×10^{11}	0.25	19.77	2.80×10^{-17}	15.70
DE-DMG-DL-TFET [23]	1.33	9.57×10^{13}	0.68	9.5	1.19×10^{-20}	70.80
SELBOX TFET [24]	46.60	5.56×10^{7}	0.6	60.73	1.00×10^{-12}	30.90
SMG JL-TFET [25]	7.50	1.19×10^{8}	0.5	80	4.30×10^{-11}	25.30
HGD-JN-TFET [26]	1.19	1.08×10^{5}	0.6	45	5.59×10^{-11}	22
SiO_2-JN-TFET [26]	0.746	5.04×10^{4}	0.74	55	6.43×10^{-11}	7.82
HIGH-K JN-TFET [26]	1.15	1.59×10^{4}	0.62	49	2.09×10^{-10}	19.10
N + POCKET SOI-DG-TFET [27]	345	2.38×10^{11}	0.38	22.21	1.26×10^{-10}	142
GAA-n-TFET [28]	5.0	2.00×10^{6}	1.1	139	1.00×10^{-11}	19.10
Si-NW-TFET [29]	0.249	4.10	0.8	79	1.50×10^{-8}	8.17
MuG pTFET [30]	0.038	3.45×10^{3}	-1.41	210	8.95×10^{-10}	3.14

Si n-i-p TFET[19]	1.40	1.4×10^{7}	−0.5	123	1.00×10^{-13}	25.00

4.5. Results for Work Done Under Objective 4

As described in Sec. 3.5, an Android mobile application titled 'BioT' has been designed, and at the time of writing this report, the application is loaded with the information which is to be made public through the application. A few screenshots of the application as taken from a mobile phone (Samsung M30s) are shown in Figure 4.41. Through this application, a user will be able to

- Understand the importance of nanocavity-in-body TFETs with special emphasis on backtrack electric field around the nanocavity-semiconductor junction.
- Access the results of the project, mapped to the three objectives.
- Establish collaborations with the PI for further enhancement of the work.
- Work on modeling aspects of electrical parameters influencing a FET-based sensor.

Figure 4.41. Screenshots of the mobile application taken on a Samsung M30s phone

5. Conclusions

The project has revealed interesting conclusions on design, simulation and modeling involving FETs and their uses as sensors. The most important ones which can significantly benefit the research community are listed here.

- In a nanocavity-in-body TFET design, the doping concentration of source needs to be lowered for improving the resolution of sensitivity among closely valued dielectric constants of biomolecules.
- A back-track electric field is discovered which opposes the front-gate electric field, and is responsible for degradation of drain current for higher dielectric constants.

- Performance of a nanocavity-in-body TFET as a sensor is better as compared to a MOSFET based gate DM MOSFET.
- TFETs with double gates on the same side of the semiconductor body can be fabricated by employing an n-p-n geometry. This reduces cost of fabrication.
- Interface reliability of n-p-n TFETs increases when a dual dielectric gate structure is used.
- The peak position of trap sensitivity for TFETs changes with workfunction or when the gate length is brought below the critical BTBT region.
- For partial hybridization (PH) of molecules in the cavity, the sensitivity degrades. For nanocavity-in-body TFETs, the sensitivity is better for positively charged molecules (FF=50%). For TFTs, the change in current sensitivity is higher for negatively charged biomolecules (FF=~46% and ~71%), although the magnitude of sensitivity is higher for positively charged biomolecules.
- Threshold voltage which is an important sensitivity parameter for FET-based sensors can be mapped to the tunneling width in case of TFETs through a linear regression model.
- A novel figure-of-merit (FOM) is developed based on electrical parameters standardized from IRDS, which can be used to assess performance of low power FETs including TFETs as sensors.

6. Scope of future work

The scope of future work is listed in points here.

- Nanocavity-in-body junctionless TFETs can be fabricated at lower cost. The absence of junctions and the need to maintain a steeper doping can relieve the designer of fabrication challenges, and emphasize on the sensitivity issues of the sensor.
- Machine learning driven models can be employed for FET-based sensor design.
- P-N junction based TFETs can be fabricated using organic semiconductors. However, stability analysis and retention of characteristics need to be investigated.
- Prospective work can be carried out on device-circuit co-design where the device segment consists of the sensor, and the circuit segment consists of the CMOS-based readout circuitry.
- Noise analysis can be extended to circuit analysis, and the impact of Random Telegraph Noise on the sensing device and the circuit can be investigated.
- More prospective designs on reducing the back-track electric field without reducing the sensitivity can be worked upon.

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Annexure-II

REQUEST FOR ANNUAL INSTALMENT WITH UP-TO-DATE STATEMENT OF EXPENDITURE

1. SERB Sanction Order No and date : SRG/ 2019/ 000660 dated 15-12-2020
2. Name of the PI : Dr. Rupam Goswami
3. Total Project Cost : Rs. 10, 49, 400
4. Revised Project Cost (if applicable) : NA
5. Date of Commencement : 9 December 2019
6. Statement of Expenditure :

(Month wise expenditure incurred during current financial year)

Month & year	Expenditure incurred/ committed
April 2022	31,000
May 2022	95,003
June 2022	11,566
July 2022	Not Applicable
August 2022	Not Applicable
September 2022	Not Applicable
October 2022	Not Applicable
November 2022	Not Applicable
December 2022	Not Applicable
January 2023	Not Applicable
February 2023	Not Applicable
March 2023	Not Applicable

1. Grant received in each year:

a. 1st Year : NIL
b. 2nd Year : Rs. 5, 24, 700 (received on 23-12-2020)
c. 3rd Year : NIL
d. 4th Year : NIL
e. Interest at the end of 2nd Year: Rs 3,558
f. Interest at the end of 3rd Year: Rs. 6,678
g. Interest at the end of 4th Year: Rs. 644
h. Total (a + b + c + d + e + f + g): Rs. 5,35,580

Statement of Expenditure

01.04.2022 to 08.06.2022 (for the financial year 2022-2023 upto end to Project)

Sl No (I)	Sanctioned Heads (II)	Total Funds Allocated (revised) (III)	Released Amount (IV)	Expenditure Incurred (Rs)				Total Expenditure till 08/06/2022 (IX=V+IV+VII+VIII)	Balance as on 08/06/2022 (X=Rs.5,35,580-IX)	Requirement of Funds upto 31st march next year	Remarks if Any
				1st Year 26.02.2020 to 31.03.2020 (V)	2nd Year 01.04.2020 to 31.03.2021 (VI)	3rd Year 01.04.2021 to 31.03.2022 (VII)	4th Year 01.04.2022 to 08.06.2022 (VIII)				
1	Manpower	7,44,000	NIL	0	0	2,01,500	70,266	2,71,766	1,36,886	-	[i]. No grant was released in the period. Therefore, total amount on 01.04.2022= Rs. 5,35,580. [ii]. Project ended on 08.06.2022 without any additional cost.
2	Consumables	0		NA	NA	NA	NA	NA			
3	Travel	1,00,000		0	0	NA	64,003	64,003			
4	Contingencies	1,00,000		0	0	NA	3,300	3,300			
5	Others (SSR)	10000		0	0	NA	NA	0			
6	Equipment	0		NA	NA	NA	NA	NA			
7	Overhead Expenses	95,400		0	0	59,625	NA	59,625			
	Total	**10,49,400**		**0**	**0**	**2,61,125**	**1,37,569**	**3,98,694**	**1,36,886**	-	

DR. RUPAM GOSWAMI
Name and Signature of Principal Investigator
Date: 14-06-2023

Signature of Competent Financial Authority
(With Seal) Finance Officer, Tezpur University
Date:

Note:

1. Expenditure under the sanctioned heads, at any point of time, should not exceed funds allocated under the head, without prior approval of SERB i.e., figures in Column (IX) should not exceed corresponding figures in Column (III).
2. Utilization Certificate (Annexure III) for financial year ending 31st March has to be enclosed along with request for carry-forward permission to the next financial year.

GFR 12 – A
[(See Rule 238 (1))]
UTILIZATION CERTIFICATE (UC) FOR THE YEAR 2022-2023
in respect of *RECURRING*
as on 08-06-2022 to be submitted to SERB
Is the UC .... *(Provisional/Audited)*
(To be given separately for each financial year ending on 31st March)

1. Name of the grant receiving Organization : ...Tezpur University......
2. Name of Principal Investigator(PI) ....Dr. Rupam Goswami....
3. SERB Sanction order no. & date ...SRG/ 2019/ 000660 dated 15-12-2020....
4. Title of the Project: ....Nanocavity-in-Body Tunnel Field Effect Transistor Architectures for Low Power Sensing Applications.........
5. Name of the SERB Scheme : Start-up Research Grant (SRG)
6. Whether recurring or non-recurring grants : ....***RECURRING***.......
7. Grants position at the beginning of the Financial year

(i)	Carry forward from previous financial year	:	Rs. 2,73,811
(ii)	Others, If any	:	NA
(iii)	**Total**	:	**Rs. 2,73,811**

8. Details of grants received, expenditure incurred and closing balances: (Actuals)

Unspent Balance of Grants received previous years [figure as at Sl. No. 7(iii)]	Interest Earned thereon	Interest deposited back to the SERB	Grants received during the year			Total Available funds (1+2-3+4)	Expenditure incurred	Closing Balances (5-6)
1	2	3	4			5	6	7
			Sanction No. (i)	Date (ii)	Amount (iii)			
Rs. 2,73,811	Rs. 644	NIL	NA	NA	NA	Rs. 2,74,455	Rs. 1,37,569	Rs. 1,36,886

Component wise utilization of grants:

Grants-in-aid- General	Grant-in-aid-creation for capital assets	Total
Rs 1,37,569	-	Rs 1,37,569

Details of grants position at the end of the year

(i)	Balance available at end of financial year (08-06-2022)	:	Rs. 1,36,886
(ii)	Unspent balance refunded to SERB (If any)	:	Rs. 1,36,886
(iii)	Balance (Carried forward to next financial year) if applicable	:	NA [End of Project on 08-06-2022]

GFR 12 – A

[(See Rule 238 (1))]

UTILIZATION CERTIFICATE (UC) FOR THE YEAR 2022-2023

in respect of *RECURRING*

as on 08-06-2022 to be submitted to SERB

Is the UC .... *(Provisional/Audited)*

(To be given separately for each financial year ending on 31st March)

Certified that I have satisfied that the conditions on which grants were sanctioned have been duly fulfilled/are being fulfilled and that I have exercised following checks to see that the money has been actually utilized for the purpose for which it was sanctioned:

(i) The main accounts and other subsidiary accounts and registers (including assets registers) are maintained as prescribed in the relevant Act/Rules/Standing instructions (mention the Act/Rules) and have been duly audited by designated auditors. The figures depicted above tally with the audited figures mentioned in financial statements/accounts.

(ii) There exist internal controls for safeguarding public funds/assets, watching outcomes and achievements of physical targets against the financial inputs, ensuring quality in asset creation etc. & the periodic evaluation of internal controls is exercised to ensure their effectiveness.

(iii) To the best of our knowledge and belief, no transactions have been entered that are in violation of relevant Act/Rules/standing instructions and scheme guidelines.

(iv) The responsibilities among the key functionaries for execution of the scheme have been assigned in clear terms and are not general in nature.

(v) The benefits were extended to the intended beneficiaries and only such areas/districts were covered where the scheme was intended to operate.

(vi) The expenditure on various components of the scheme was in the proportions authorized as per the scheme guidelines and terms and conditions of the grants-in-aid.

(vii) It has been ensured that the physical and financial performance under ....SRG.... has been according to the requirements, as prescribed in the guidelines issued by Govt. of India and the performance/targets achieved statement for the year to which the utilization of the fund resulted in outcomes given at Annexure – I duly enclosed.

(viii) The utilization of the fund resulted in outcomes given at Annexure – II duly enclosed (to be formulated by the Ministry/Department concerned as per their requirements/specifications.)

(ix) Details of various schemes executed by the agency through grants-in-aid received from the same Ministry or from other Ministries is enclosed at Annexure –II (to be formulated by the Ministry/Department concerned as per their requirements/specifications).

Date:

Place: Tezpur University

Signature of PI :	Signature with Seal :................. Name: .... Chief Finance Officer (Head of Finance) Finance Officer Tezpur University	Signature with Seal....................... Name: .... Registrar Head of Organisation Tezpur University

SERB Start-up Research Grant **27 February 2023**
File No. SRG/2019/000660

Since there was no non-recurring budget head sanctioned for the project, therefore, no UC is uploaded for non-recurring budget.

Rupam Goswami
(RUPAM GOSWAMI)
Principal Investigator

Enclosed: Sanction Letter for the project

A

FILE NO. SRG/2019/000660

SCIENCE & ENGINEERING RESEARCH BOARD(SERB)

(a statutory body of the Department of Science & Technology, government of India)

5 & 5A, Lower Ground Floor
Vasant Square Mall
Plot No. A, Community Centre
Sector-B, Pocket-5, Vasant Kunj
New Delhi-110070

Dated: 15 December, 2020

ORDER

Subject: Research project entitled **"Nanocavity-in-Body Tunnel Field Effect Transistor Architectures for Low Power Sensing Applications"** under the guidance of Dr. RUPAM GOSWAMI, Electronics and Communication Engineering, Tezpur University , Napaam, tezpur, assam, Tezpur, Assam-784028.

1. This is in continuation of SERB's sanction order No. "SRG/2019/000660" dated "26 November, 2019 " of **Science and Engineering Research Board (SERB)**.
The budget for both the institutes is given below:

S. No	Head	Original Total Cost (in INR)	Allocation for Birla Institute of Technology and Science (BITS)-Pilani Campus, Pilani Campus, Vidya Vihar, Pilani (in INR)	Allocation for Tezpur University, Napaam, Tezpur, Assam (in INR)	Revised Budget (in INR)
A	**Non-recurring (Capital Items)**				
1	Equipment	0	0	0	0
A'	*Total - Capital*	***0***	***0***	***0***	***0***
B	**Recurring Items**				
1	Manpower *-> Junior Research Fellow - 1[(Rs. 372000/- PY for I year , Rs. 372000/- PY for II year)]*	744000	0	744000	744000
2	Consumables	0	0	0	0
3	Travel	100000	0	100000	100000
4	Contingencies	100000	0	100000	100000
5	Other Cost.	0	0	0	0
6	Scientific Social Responsibility	10000	0	10000	10000
	General - I (Manpower, Consumables, Travel, Contingencies, Other Cost, SSR)	954000	0	954000	954000
	General - II Overhead Charges	95400	0	95400	95400
B'	*Total - Recurring*	***1049400***	***0***	***1049400***	***1049400***
C	**Total cost of the project (A' + B')**	**1049400**	**0**	**1049400**	**1049400**

2. The revised total cost of the project at **Birla Institute of Technology and Science (BITS)-Pilani Campus, Pilani Campus, Vidya Vihar, Pilani** would be Rs. 0/- and total cost for **Tezpur University, Napaam, Tezpur, Assam** would be Rs. 1049400/- The project duration is till 08 December, 2021.

3. Sanction of the competent authority is hereby accorded to the payment of a sum of **Rs. 524700/-** (Rupees Five Lakh Twenty Four Thousand Seven Hundred only) under 'Grants-in-aid General' to **REGISTRAR, Tezpur University, Napaam, Tezpur, Assam** being the 2nd grant for the financial year 2020-2021 for implementation of the above said project.

4. Sanction of the competent authority is also accorded to the transfer of unspent balance of **Rs. 0/-** (Rupees only) (Recurring Rs. 0 and Non-Recurring Rs. 0) to Tezpur University, Napaam, Tezpur, Assam from FY 2019-2020 to FY 2020-2021 for the same purpose for which it was sanctioned .

5. Sanction of the grant is subject to the conditions as detailed in Terms & Conditions available at the website (www.serb.gov.in).

6. It is certified that provision of GFR 212 relating to Utilization Certificates (Ucs) for the funds released under the grant have been satisfied and the UC/s is/are enclosed herewith.

7. The expenditure involved is debitable to **Fund for Science & Engineering Research (FSER)** **This release is being made under Start-up Research Grant. (EC Engineering Sciences)**

8. The Sanction has been issued to Tezpur University, Napaam, Tezpur, Assam with the approval of the competent authority under delegated powers on **20 October, 2020** and vide Diary No. **SERB/F/4575/2020-2021** dated **28 October, 2020**

9. The release amount of **Rs. 524700/-** (Rupees Five Lakh Twenty Four Thousand Seven Hundred only) (Recurring Rs. 524700 and Non-Recurring Rs. 0) will be drawn by the Under Secretary of the SERB and will be disbursed by means of RTGS transaction as per their Bank details given below:

PFMS Unique Code	TU
Account Name	TEZPUR UNIVERSITY R&D
Account Number	30448821505
Bank Name & Branch	STATE BANK OF INDIA TEZPUR UNIVERSITY BRANCH, ASSAM 784028
IFSC/RTGS Code	SBIN0014259
Email id of A/C Holder	registrartu@tezu.ernet.in
Email id of PI	rup.gos@gmail.com

10. The institute will maintain separate audited accounts for the project. A part or whole of the grant must be kept in an interest earning bank account which is to be reported to SERB. The interest thus earned will be treated as credit to the institute to be adjusted towards further installment of the grant.

11. As per rule 211 of GFR the accounts of Grantee Institution shall be open to inspection by the sanctioning authority / audit whenever the institute is called upon to do so.

12. The institute will furnish to the SERB, Utilization certificate(separate for Recurring & Non-Recurring) and an audited statement of accounts pertaining to the grant immediately after the end of each financial year.

13. After completion of the project unspent balance if any should be returned as Demand Draft drawn in favour of "Fund for Science and Engineering Research" payable at New Delhi.

14. The organization/institute/university should ensure that the technical support/financial assistance provided to them by the Science & Engineering Research Board, a statutory body of the Department of Science & Technology (DST), Government of India should invariably be highlighted/ acknowledged in their media releases as well as in bold letters in the opening paragraphs of their Annual Report.

15. In addition, the investigator/host institute must also acknowledge the support provided to them in all publications, patents and any other output emanating out of the project/program funded by the Science & Engineering Research Board, a statutory body of Department of Science & Technology (DST), Government of India.

16. The File no. SRG/2019/000660 may also be mentioned in all research communications arising from the above project with due acknowledgement of SERB.

17. As this is the first grant to the **Tezpur University, Napaam, Tezpur, Assam** for the fellowship, no previous U/C is required.

(Dr. Ramesh Vijayan)
Scientist - D
drvramesh@serb.gov.in

To,
Under Secretary
SERB, New Delhi

Copy forwarded for information and necessary action to: -

1.	The Principal Director of Audit, A.G.C.R.Building, IIIrd Floor I.P. Estate, Delhi-110002
2.	Sanction Folder, SERB , New Delhi.
3.	File Copy
4.	**Dr. RUPAM GOSWAMI** **Electronics and Communication Engineering** **Tezpur University , Napaam, tezpur, assam, Tezpur, Assam-784028** **Email: rup.gos@gmail.com** **Mobile: 919864803577**
5.	**REGISTRAR,** **Tezpur University, Napaam, Tezpur, Assam**
6.	**Director,** **Birla Institute Of Technology And Science (BITS)-Pilani Campus, Pilani Campus,** Vidya Vihar, **Pilani**

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